Future Trends of Non Volatile Memory Technology

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December 2001

Agenda

- Scaling trend of ETOX® NOR Flash
- Multi-level and multi-bit technologies
- Internet on a chip technology
- Next generation memory technologies
- Ovonics unified memories for code + data storage
- Summary

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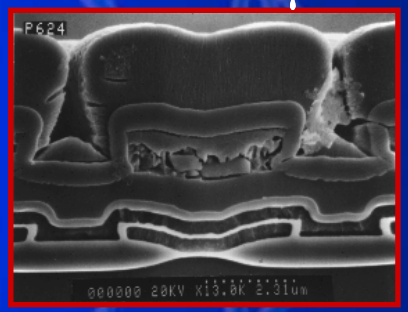
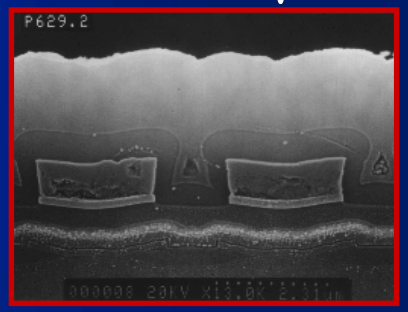
ETOX® Technology Scaling

- 18 years and 8 Generations of ETOX® to 0.13 µm

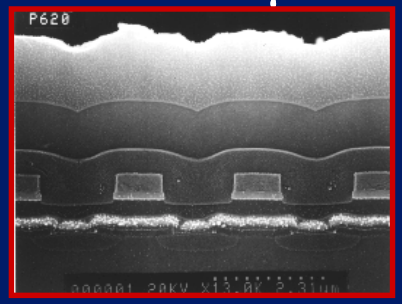
1986 / 1.5µm



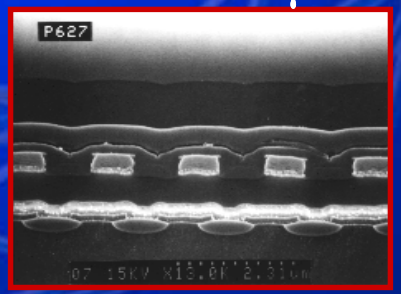
1988 / 1.0µm



1991 / 0.8µm



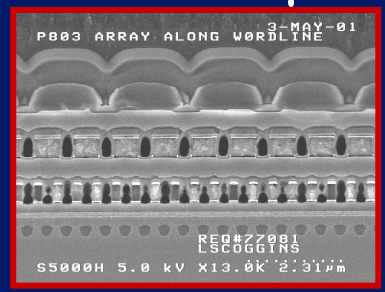
1993 / 0.6µm



1996 / 0.4µm

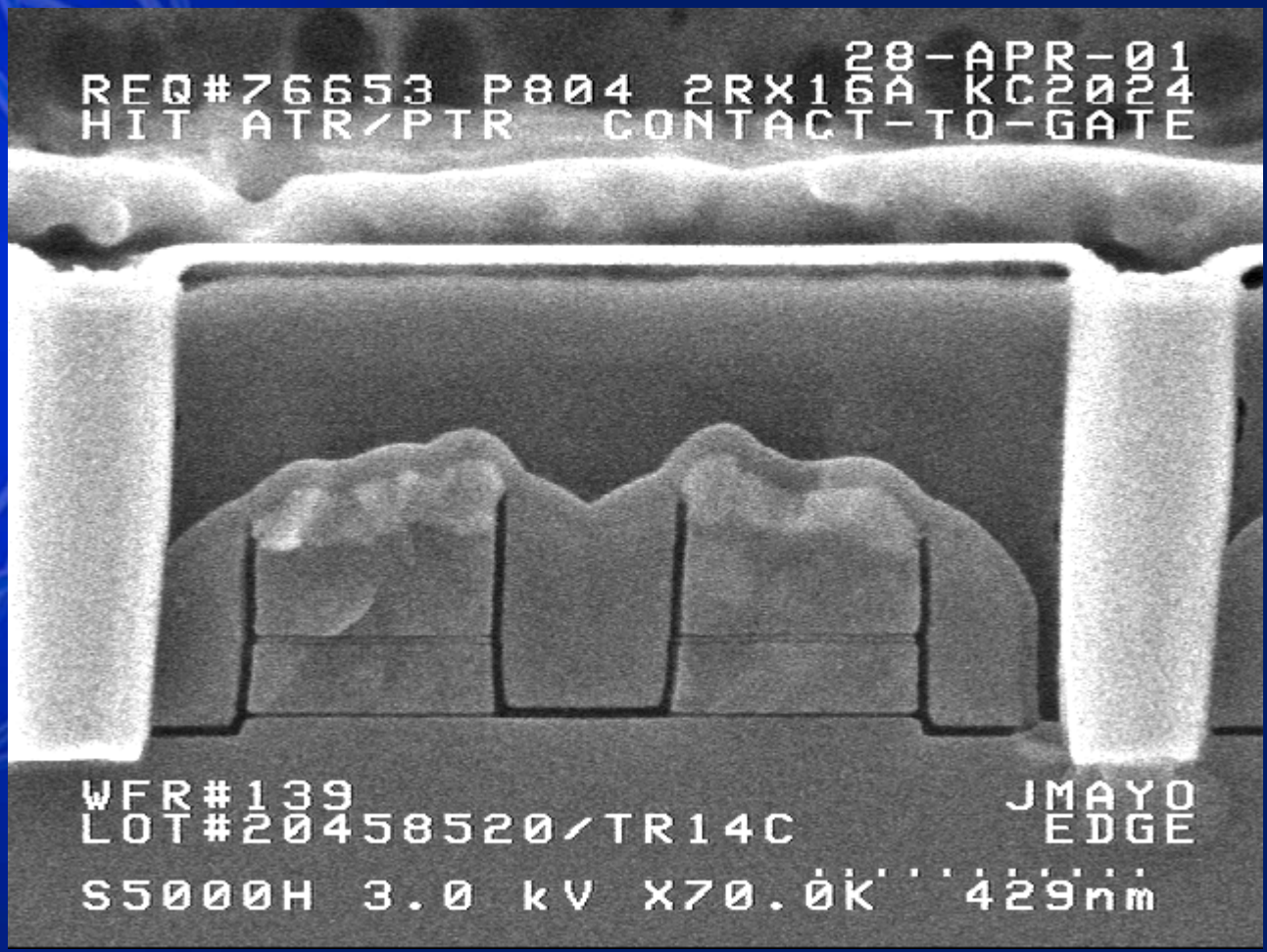
1998 / 0.25µm

2000 / 0.18µm

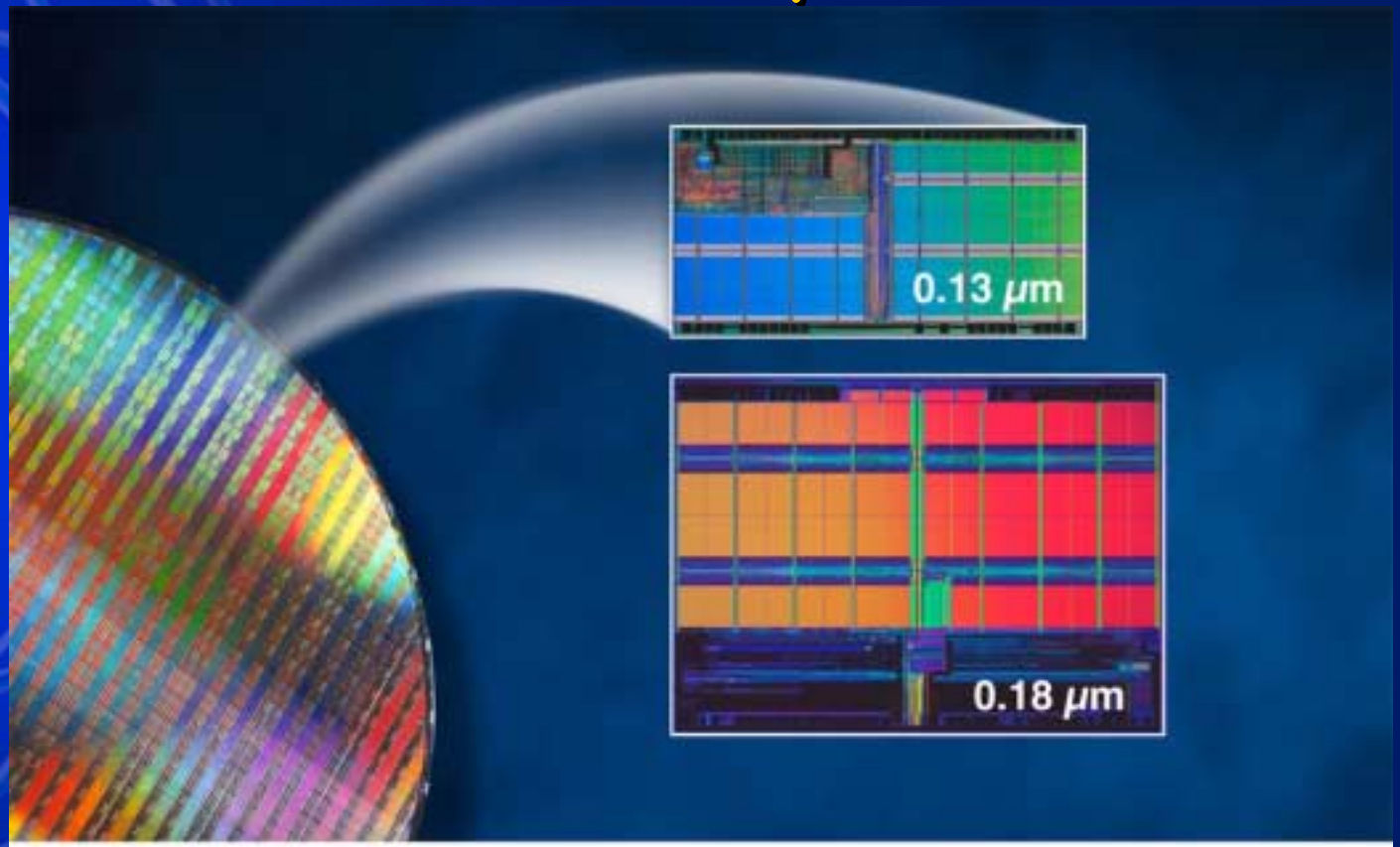


Volume Production Year / Technology Generation

0.13 µm ETOX® Flash Memory Cell



Die Size Reduction at 0.13 µm



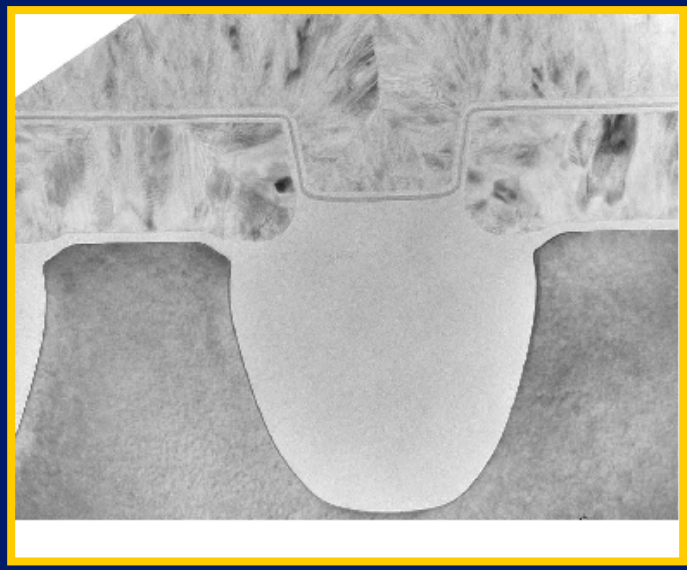
Intel® Advanced+ Boot Block is the world's first flash memory to ship on 0.13-micron lithography. The smaller size of the 0.13 µm die, shown here in comparison to the 0.18 µm process die, will add increased density, functionality and performance.

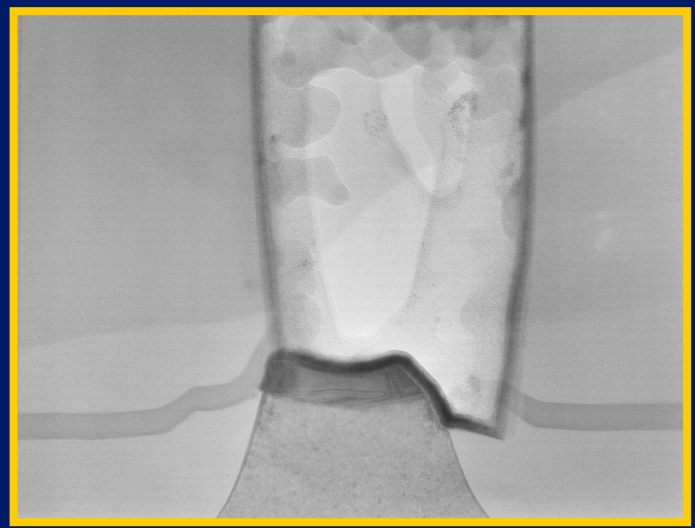
ETOX® Cell Scaling

- ETOX® NOR Cell has two scaling limiters:
  - Stressed induced charge loss limits tunnel oxide thickness to >80 nm
  - Channel hot electron programming limits internal voltage to >8 volts
- Scaling so far driven by lithography and feature innovation
  - Leff and Zeff scales slower
  - Most cell size reduction through “dead space” reduction

ETOX® Technology Innovation

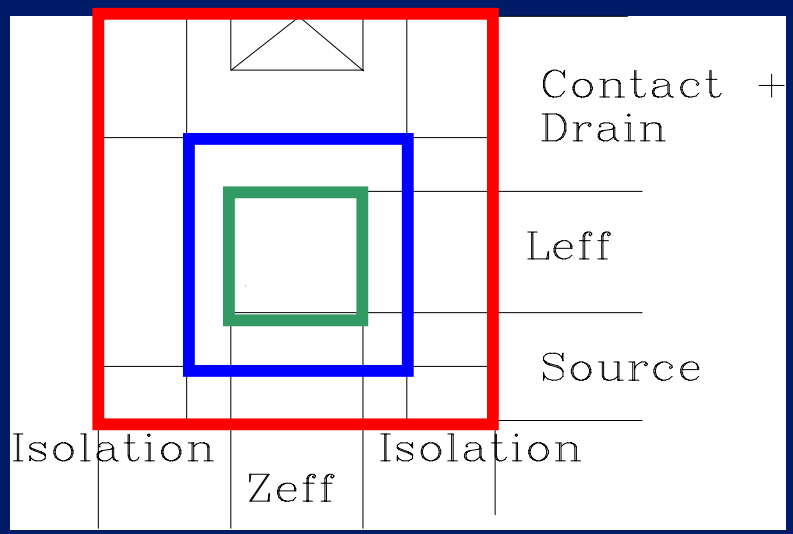
Generation	Innovations
0.25 µm	• Trench Isolation • Salicide
0.18 µm	• Self Aligned Poly • Unlanded Contacts • Triple Well • High Performance Transistors • Three Layers of Metal
0.13 µm	• Channel Erase
90 nm	• To be determined
65 nm	• To be determined

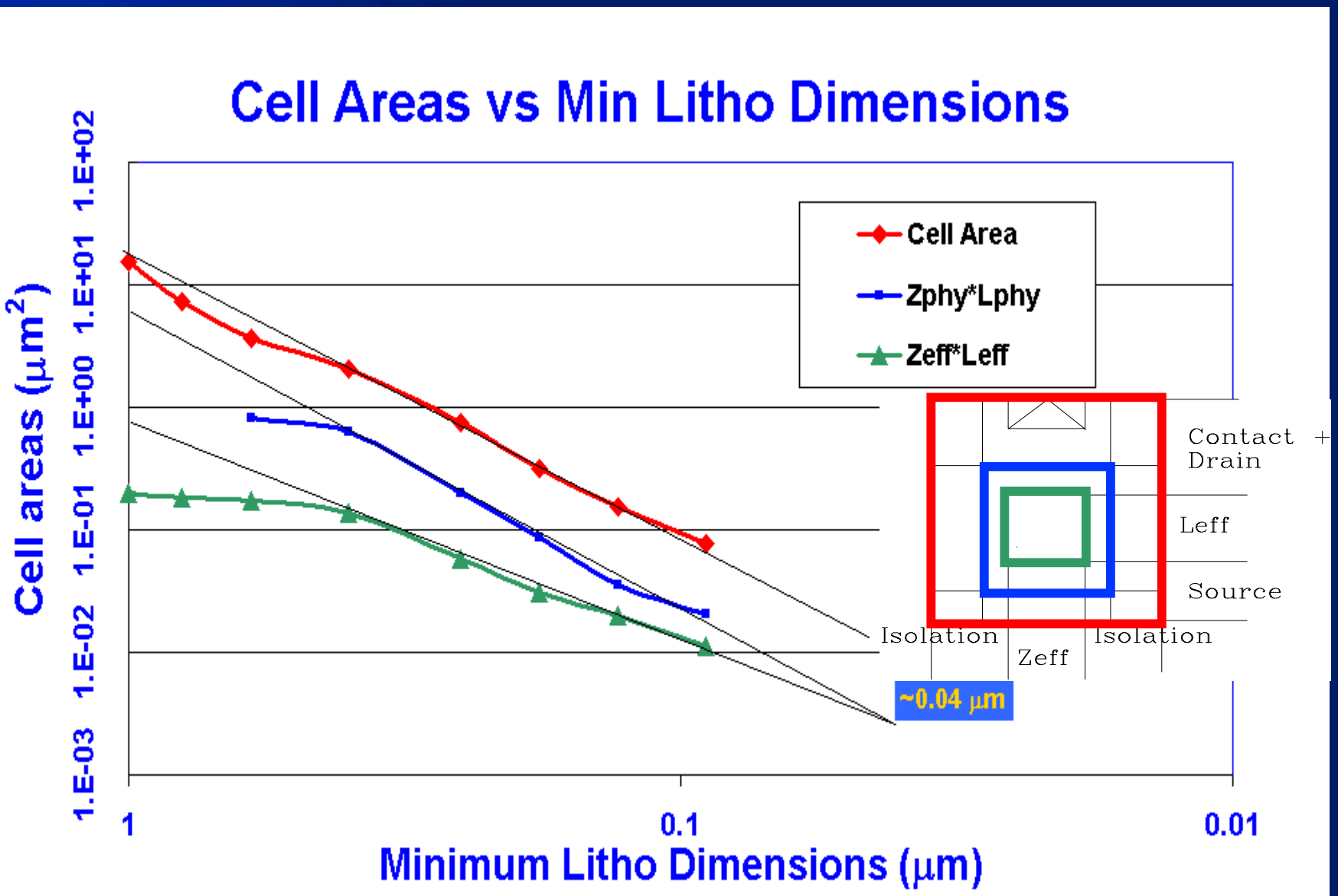




Scaling Limit Extrapolation

- Zeff and Leff are the minimum electrical dimensions and scale slowly
- Zphy and Lphy = minimum physical dimensions defined by lithography or cell requirement
- Zphy-Zeff=isolation beak
- Lphy-Leff=source/drain underlap
- Beak and source/drain underlap are scaled but cannot be zero
- Extrapolation of intercept at 40 nm node represents scaling limit
- Practical limit 65 nm node for planar cell, new cell structure like 3D cell will be needed at 40 nm node




Cell Areas vs Min Litho Dimensions
Cell areas (μm²)
1.E-03
1.E-02
1.E-01
1.E+00
1.E+01
1.E+02
Cell Area
Zphy*Lphy
Zeff*Leff
Contact + Drain
Leff
Source
Isolation
Zeff
Isolation
~0.04 μm
1
0.1
0.01
Minimum Litho Dimensions (μm)

Scaling Limit Extrapolation

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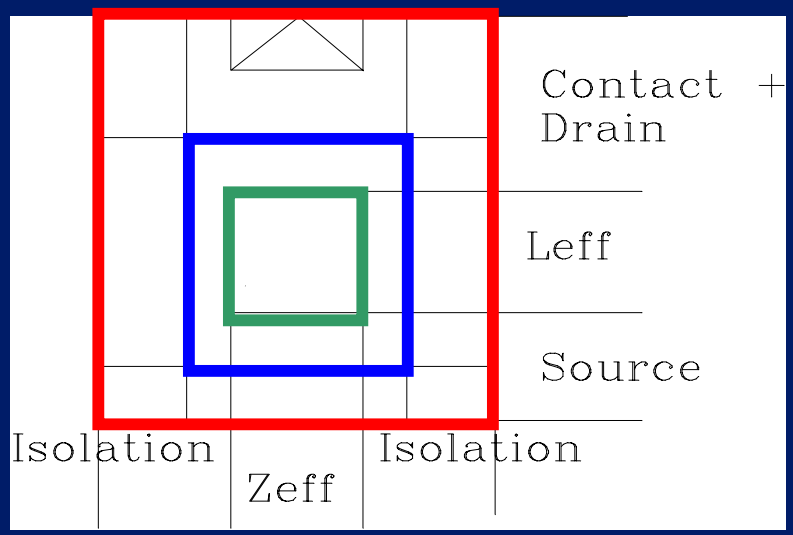

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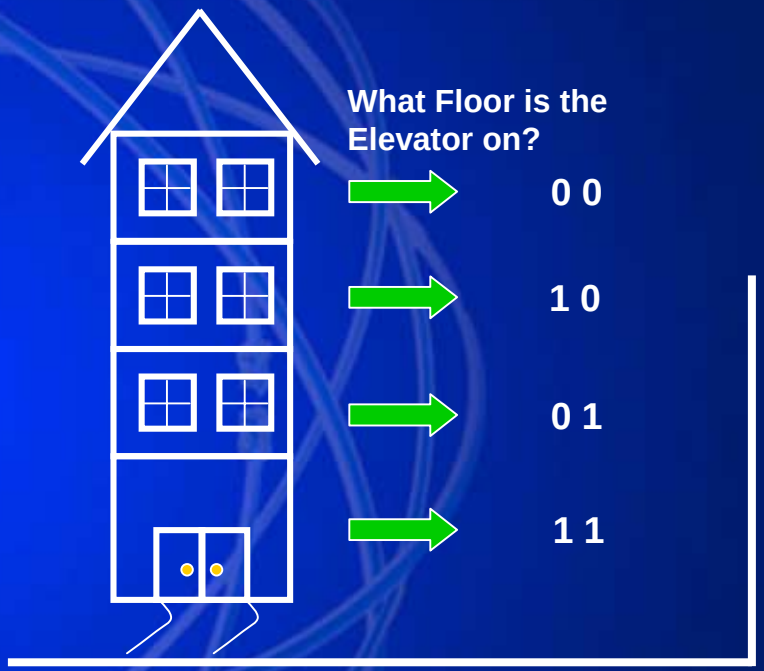
Multi-level and Multi-bit Technologies

- To reduce memory cost further, techniques are developed to store more than one bit of information per cell
- Multi-level (Intel StrataFlash® Memory) technology was first developed: over 2 billion Mbits shipped so far
- Multi-bit technologies have been reported recently

Multi-Level Cell & Multi-Bit Concepts

Multi-Level Cell



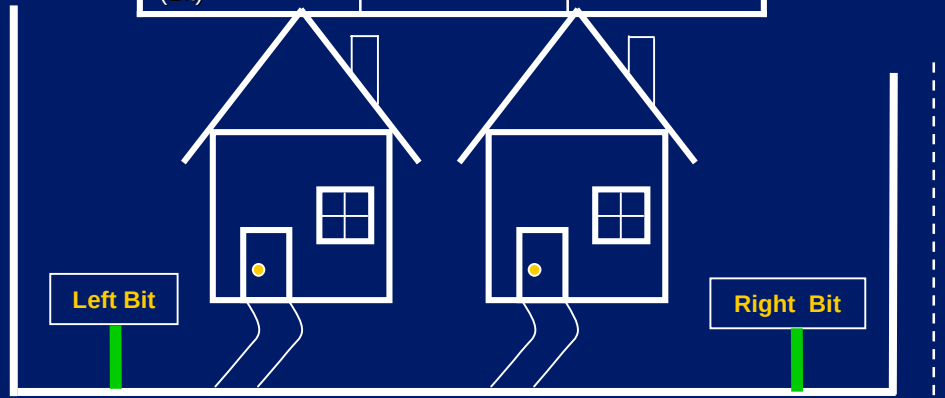
Flash Cell: 4 Story Office Building

What Level?

Multi-Bit Cell

Which House?…….And Is Anybody Home?

Which House?	Any Body Home? (Pgm or Erase)	
	Yes	No
Left House (Bit)	1	0
Right House (Bit)	1	0

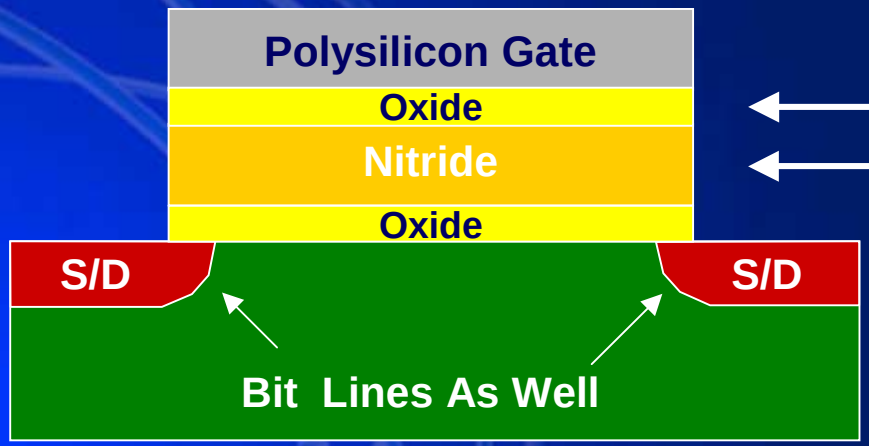


Flash Cell: 2 Residence Street

Which Bit *and* What's Its State?

Memory Cell Structures

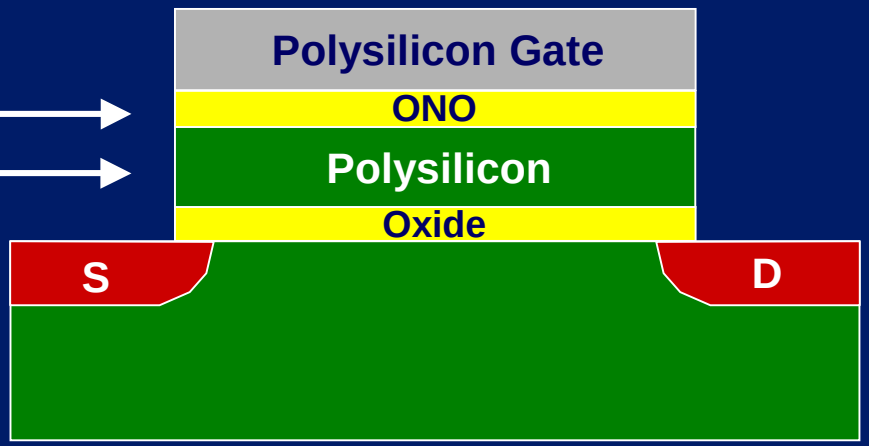
Multi-bit



- NMOS Device
- Nitride Floating Gate
  - Trap Based Charge Storage
- Virtual Array Ground

Entirely <u>Different</u> From Current Single Bit Per Cell Technology: New Learning required, Immature

StrataFlash® Memory



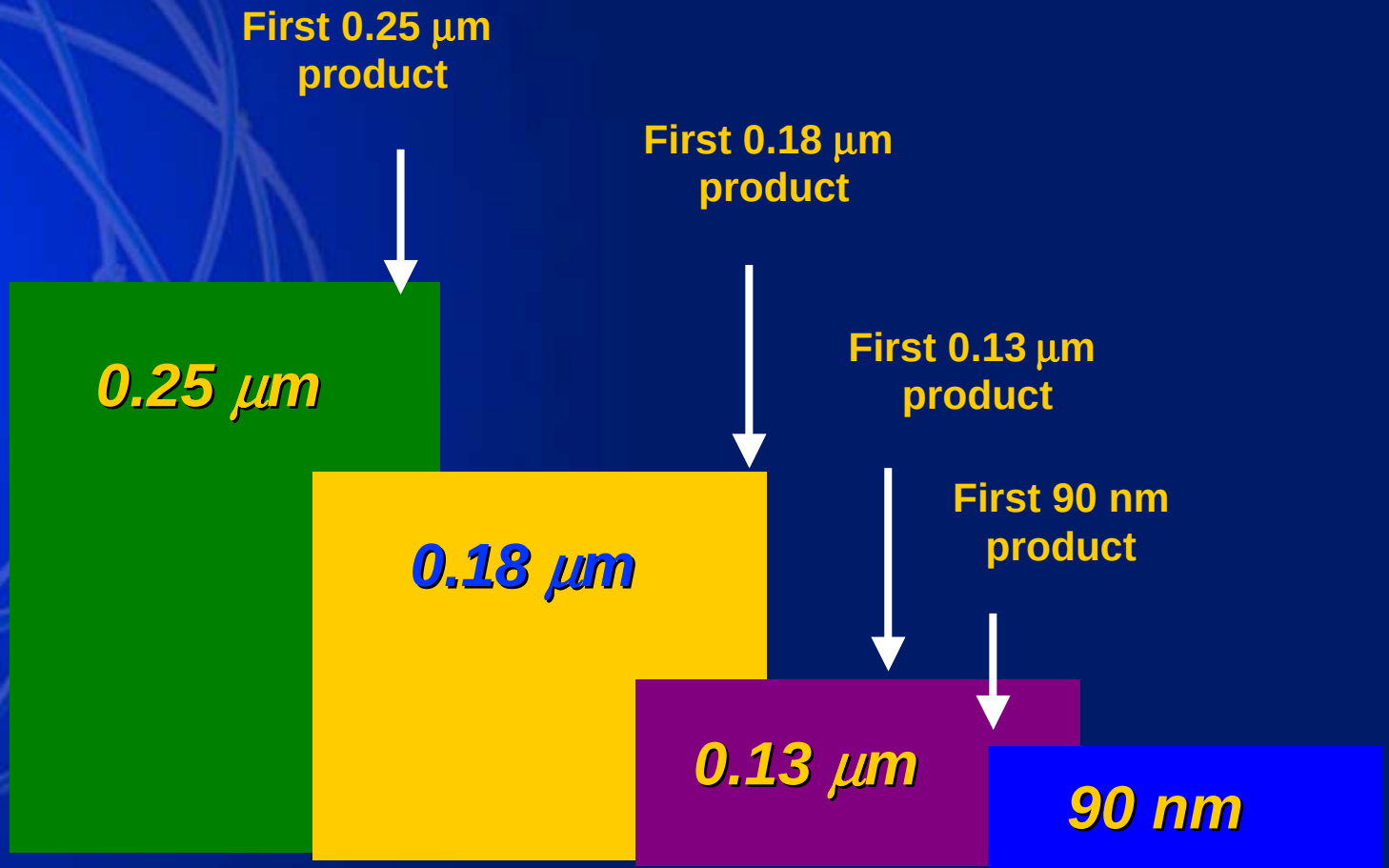
- NMOS Device
- Polysilicon Floating Gate
  - Conductive Based Charge Storage
- Solid Array Ground

<u>Same</u> Single Bit Per Cell Technology: Leverage High Volume Product Learning

Multi-Level vs Multi-Bit

Multi-Level	Multi-Bit
Floating Gate Storage, Charge Distributed, Oxide Defect Fatal	Nitride Storage, Charge Localized, Local Defect OK
Channel Hot Electron Program, Tunnel Oxide Erase, No Location Sensitivity	Channel Hot Electron Program, Tunnel Oxide Local Erase, Program/erase location critical
More Process Steps Proven Yield	Less Process Steps Yield Not Proven
>2000 electrons at 0.25 μm generation	<2000 electrons at 0.25 μm generation
Proven Reliability	Unproven Reliability
2 Billion Mbits Shipped since 1997	?

Pulling in StrataFlash® Memory Product Schedules



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Internet on a Chip Technology

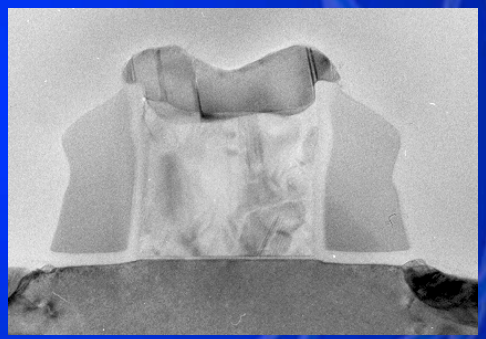
- With the scaling of logic, flash and analog technologies, it is economical to combine all the technologies– without compromising performance or density – onto a single chip using one manufacturing process.
- One can combine the core components of today's cell phones and handheld computers onto a single chip.
- Chips produced on the new process may be up to five times more powerful than today's wireless devices.

Logic Technology Scaling

- Driving Moore's Law

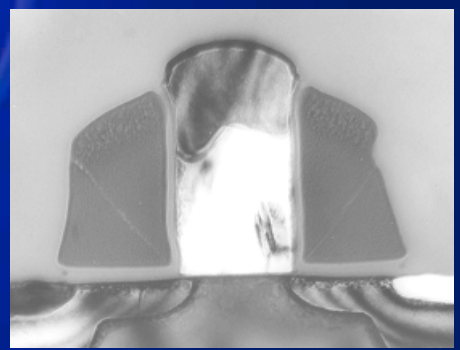
Production Volume Year

1H97



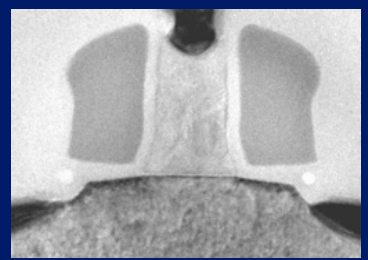
0.20µm

1H99



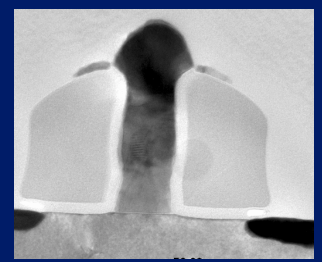
0.13µm

2001



~0.07µm

2003



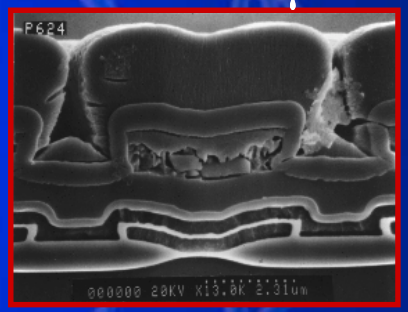
~0.05µm

Gate width

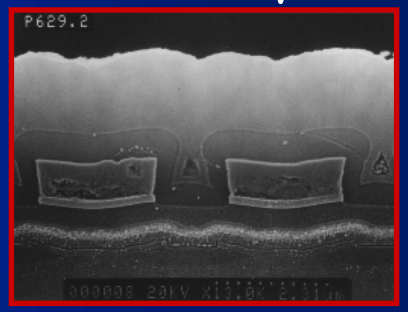
ETOX® Technology Scaling

- 18 years and 8 Generations of ETOX® to 0.13 µm

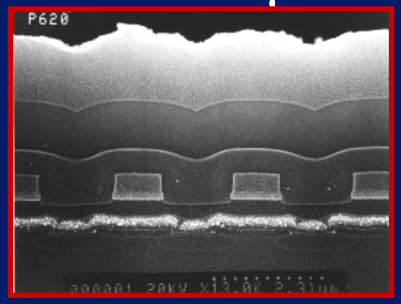
1986 / 1.5µm



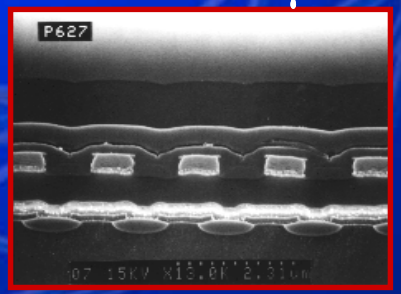
1988 / 1.0µm



1991 / 0.8µm



1993 / 0.6µm



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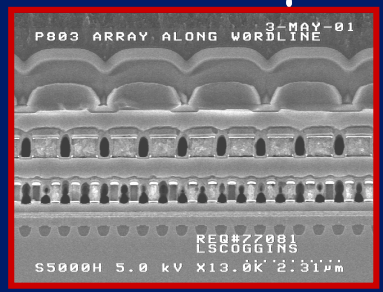


Volume Production Year / Technology Generation

Intel's Wireless Personal Internet Client Architecture: PCA

- PCA Silicon hardware building blocks meeting the convergence needs of voice + data.
- Building Blocks: Compute, Communications and Memory
  - Silicon Processing: Some common process technology steps, common fabrication facility, separate wafers.

Compute

Intel® XScale™ Microarchitecture

Communications

Intel Baseband chipsets With Intel® Micro Signal Architecture

Memory

Intel® Flash Memory

"Wireless-Internet-on-a-Chip" Technology

- Intel is able to integrate it's leadership logic, flash and analog silicon technologies onto the same silicon, without compromising performance or density, providing leadership "System-on-a-Chip" capabilities.
  - Silicon Processing: Exact same process technology steps, same fabrication facility, same wafer → leadership integrated components.

Compute

Intel® XScale™ Microarchitecture

Memory

Intel® Flash Memory

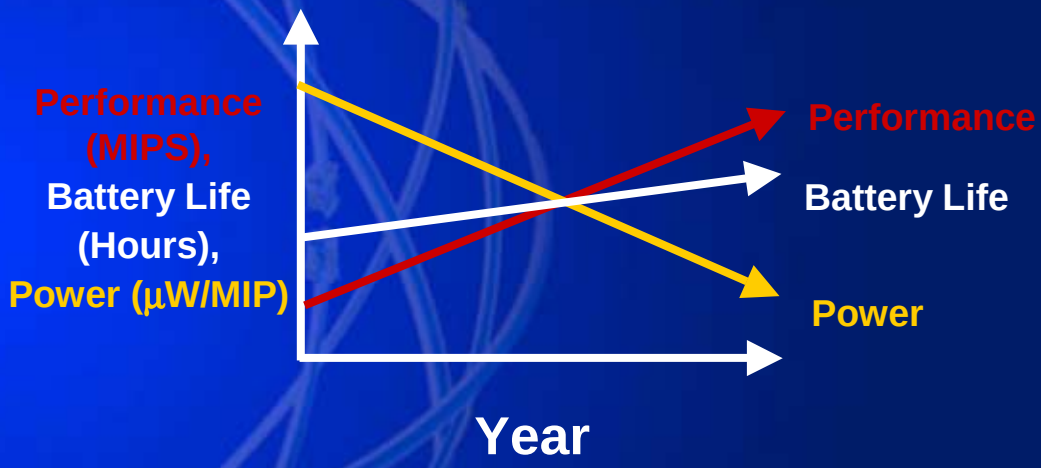
Communications

Intel Baseband chipsets With Intel® Micro Signal Architecture

Wireless Internet on a Chip

Advantage of Silicon Integration

Converged Voice + Data Requirements Trend



Flash + Logic + Analog Integration

High Performance with Memory & Compute Integration

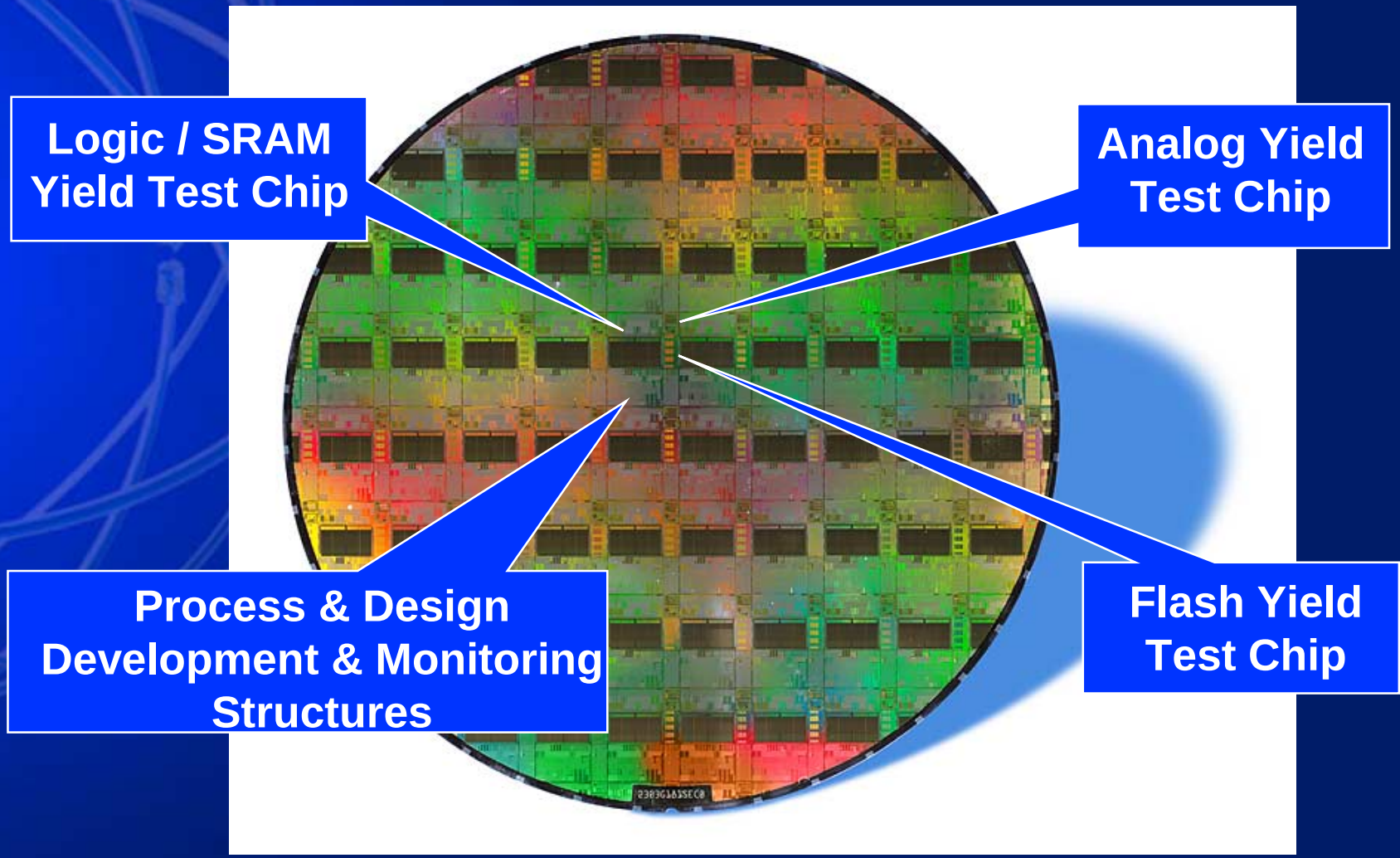
Low Power with elimination of external busses

Improved MIPs/µW → Longer Battery Life

Small form factor & improved reliability with fewer components

“Wireless Internet on a Chip”

- Integrated Flash + Logic + Analog Demonstrated



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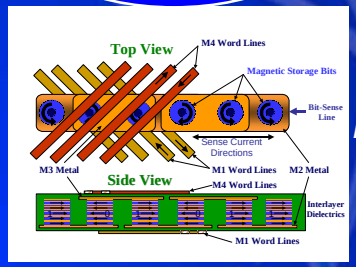
Need for Next-Gen Memories

- Industry searching for future memory technologies for portable devices (cell phones, mobile PCs, etc.)
  - Desired memory attributes: Low cost, low power, non-volatile and easy to integrate
- Today's memory technologies each have limitation(s)
  - DRAM is volatile and difficult to integrate
  - SRAM is high cost and volatile
  - Flash has slower writes and ~1 million write/erase cycles
- Several next-generation memory technologies are being studied, including MRAM, FeRAM, Polymer Memory and Ovonics Unified Memory (OUM)

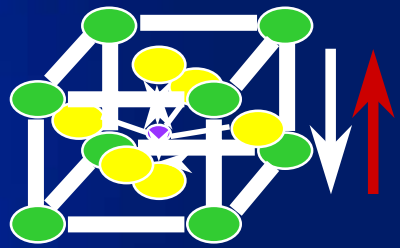
More New Technologies Than Any Time In History

MRAM

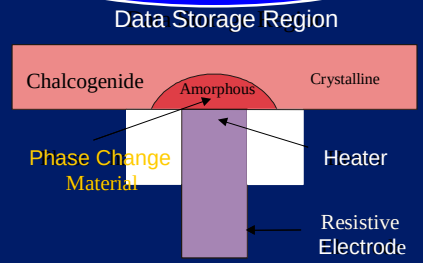


Applied Electric Field Moves Center Atom

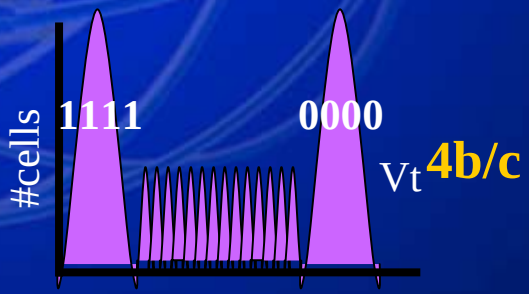
FERAM



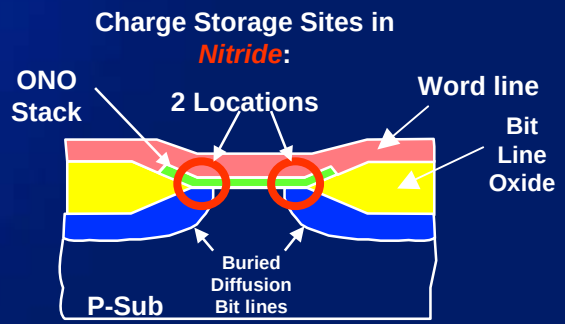
OUM



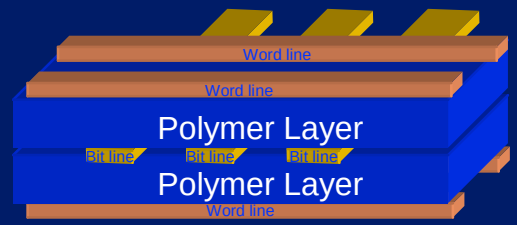
ETOX®-4bpc



NROM



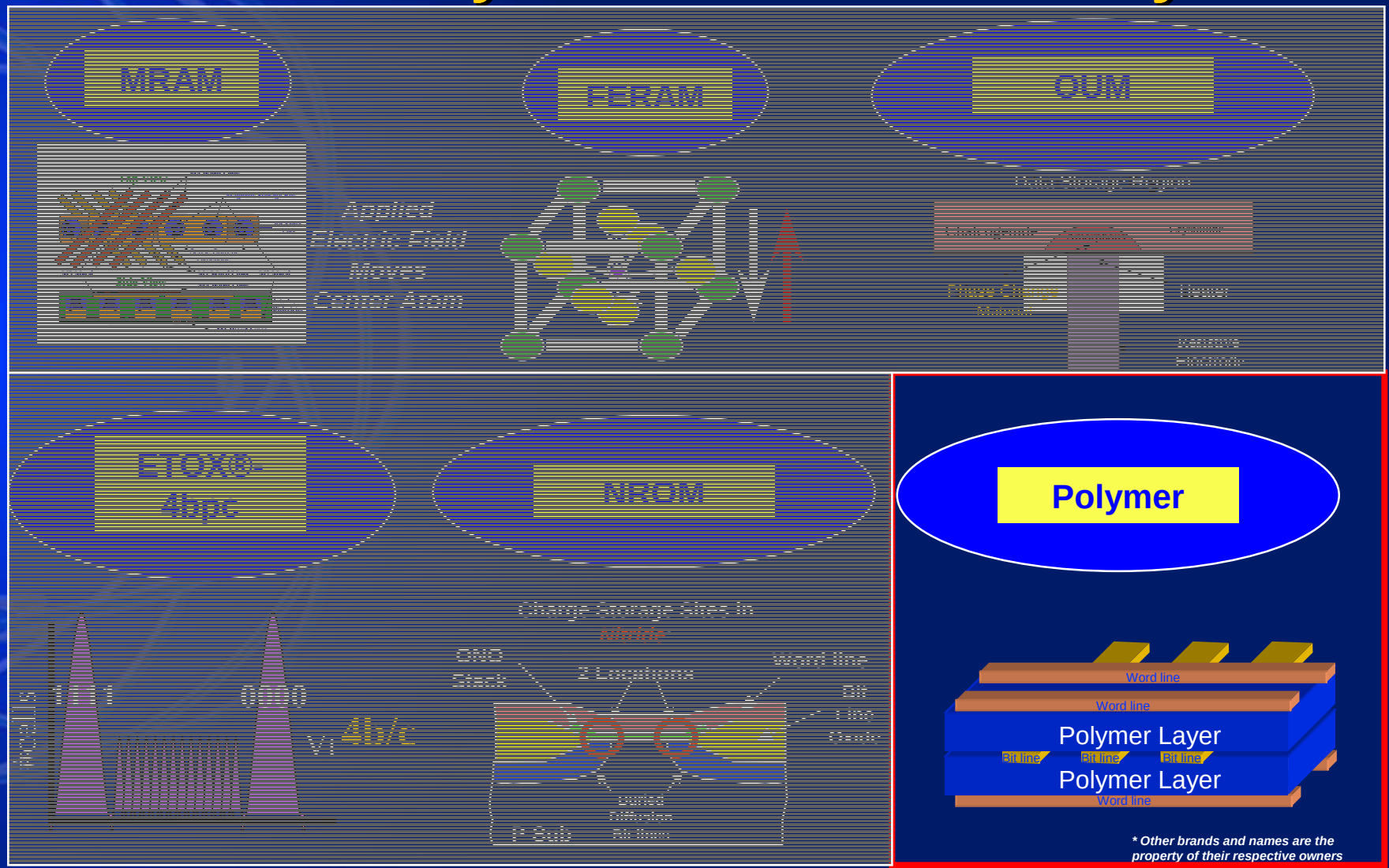
Polymer



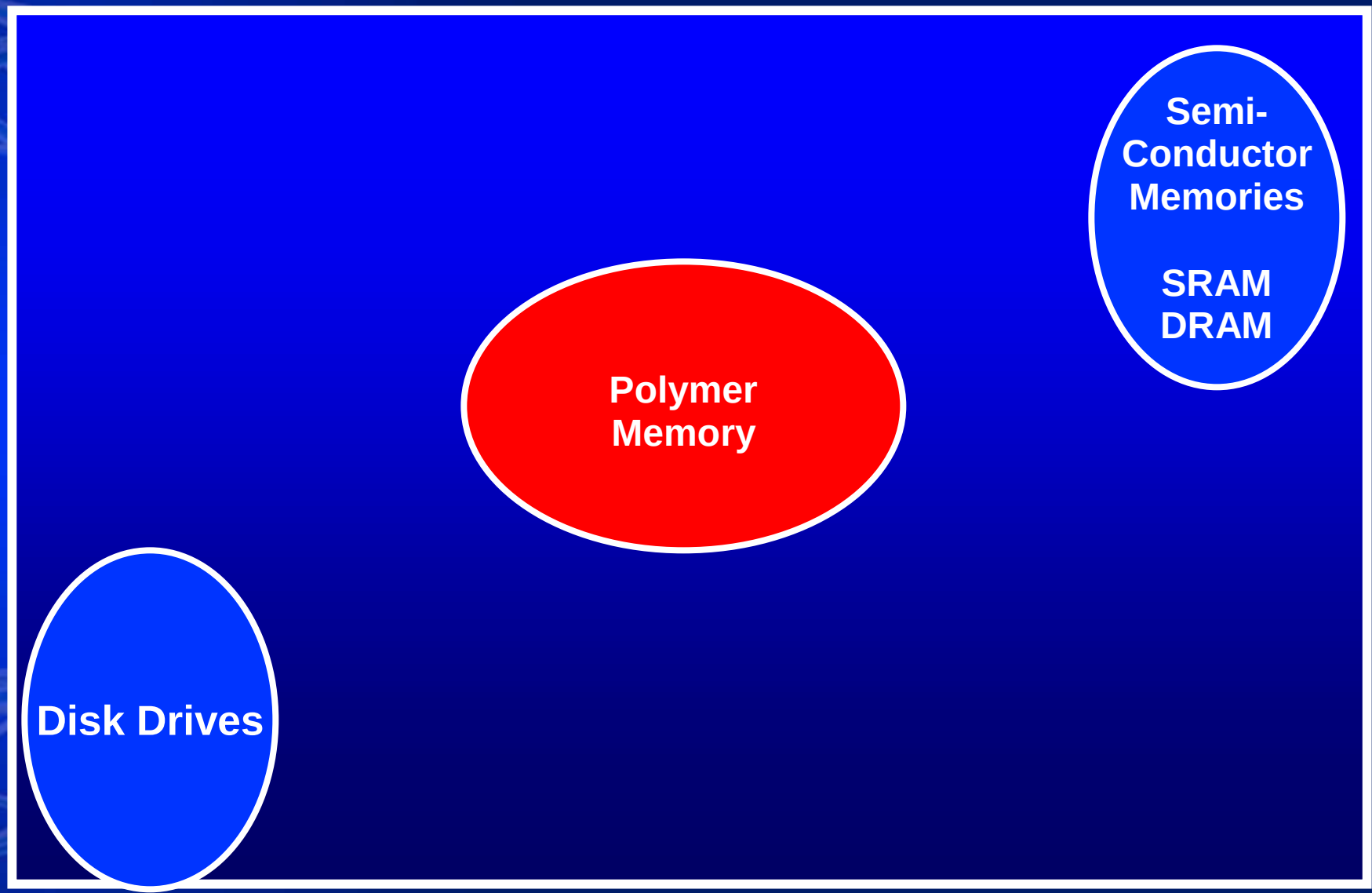
** Other brands and names are the property of their respective owners*

One or two will become mainstream

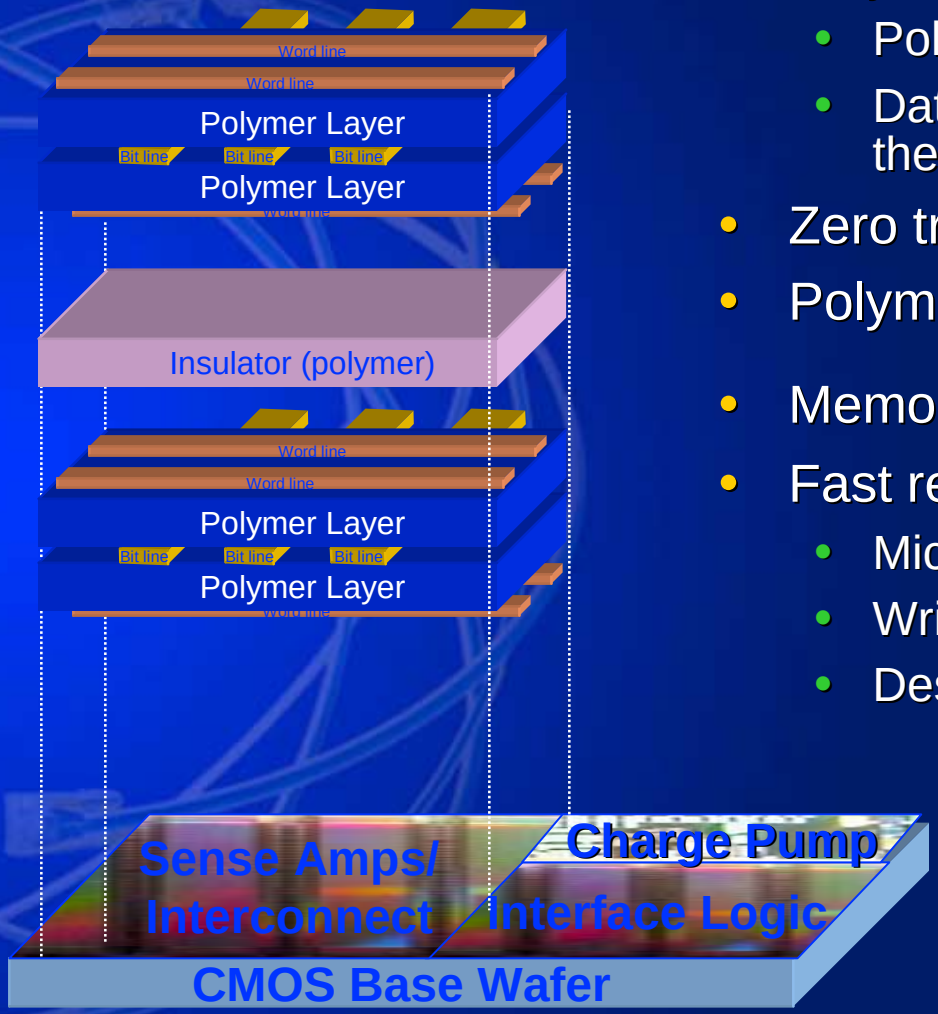
More New Technologies Than Any Time In History



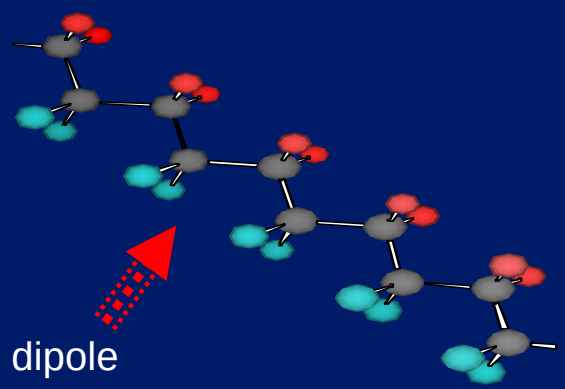
Value of Polymer Memory



What Is Polymer Memory?



- Polymeric Ferroelectric RAM (PFRAM)
  - Polymer chains with a dipole moment
  - Data stored by changing the polarization of the polymer between metal lines
- Zero transistors per bit of storage
- Polymer layers can be stacked
- Memory is NON-Volatile
- Fast read and write speeds
  - Microsecond initial reads
  - Write speed comparable to flash
  - Destructive read

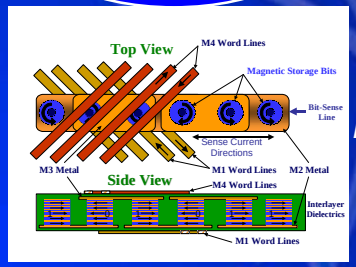


Attributes of Polymer Memory

- Very low cost/bit, high capacity per dollar
  - Simple processing, easy to integrate with other CMOS
  - $4\lambda^2$ cell size is effectively $\frac{1}{2}\lambda^2$ with 8 layers stacked (vs. 3 λ^2 for 2 bit/cell NAND)
- Low power consumption
  - No cell standby power or refresh required
- PFRAM low-cost/high capacity fits well in handheld data storage applications

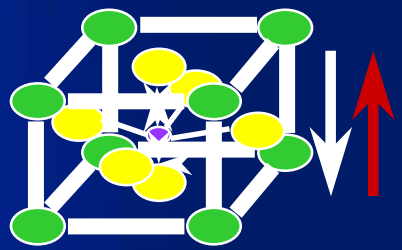
More New Technologies Than Any Time In History

MRAM

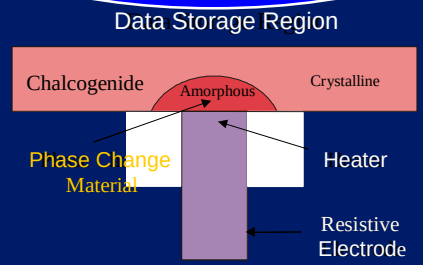


Applied Electric Field Moves Center Atom

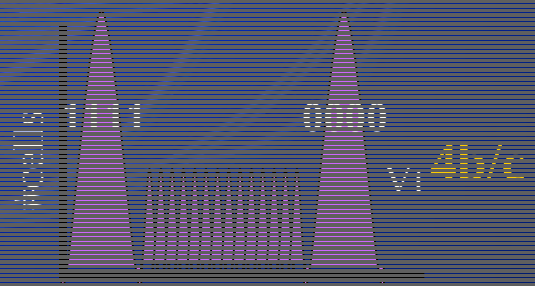
FERAM



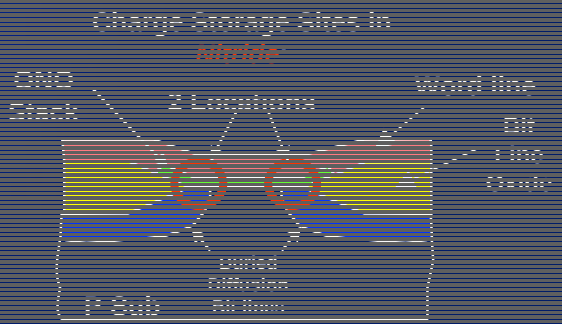
OUM



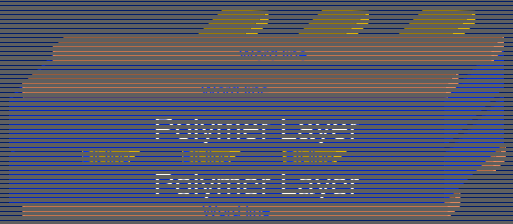
ETOX®-4bpc



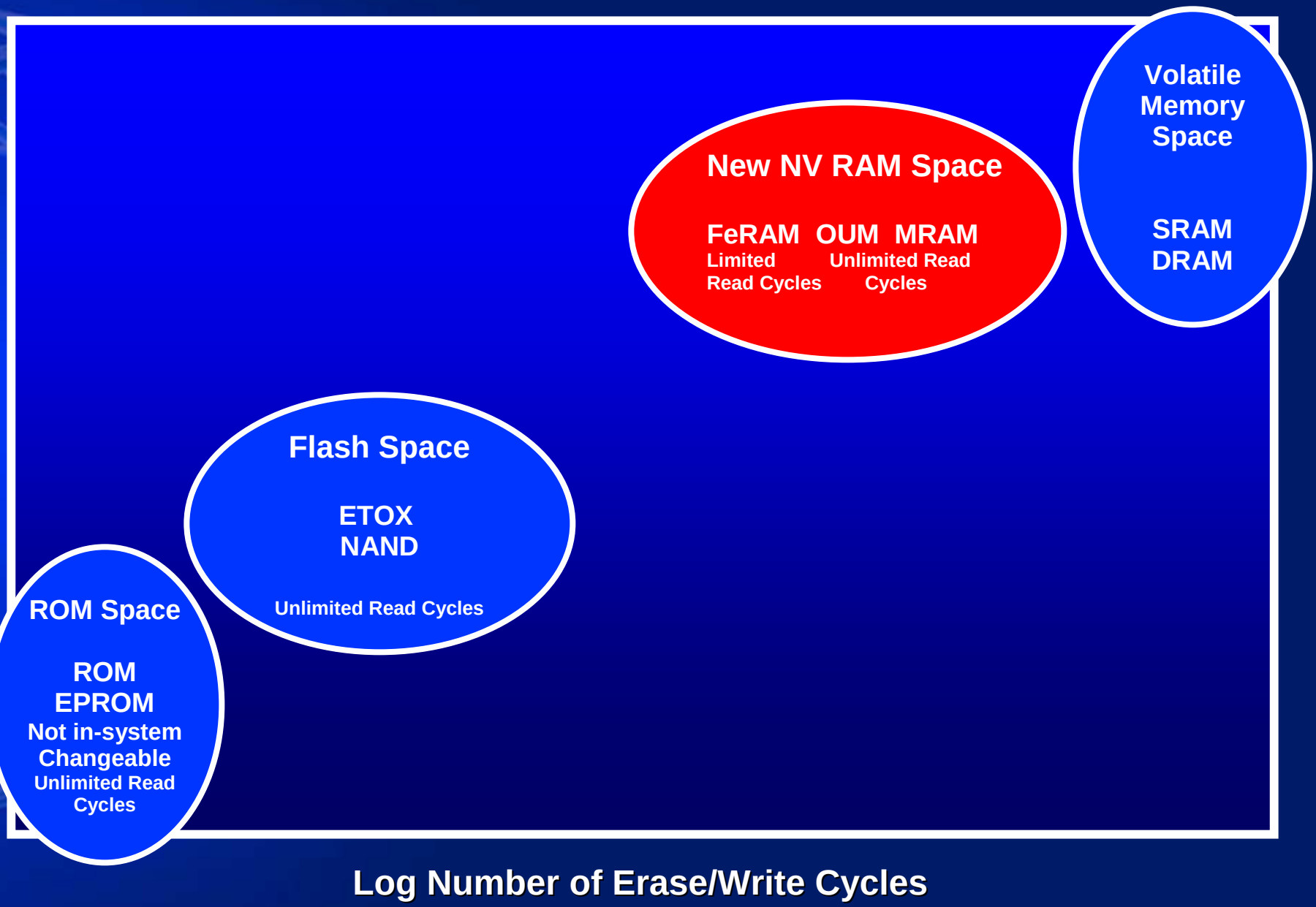
NROM



Polymer

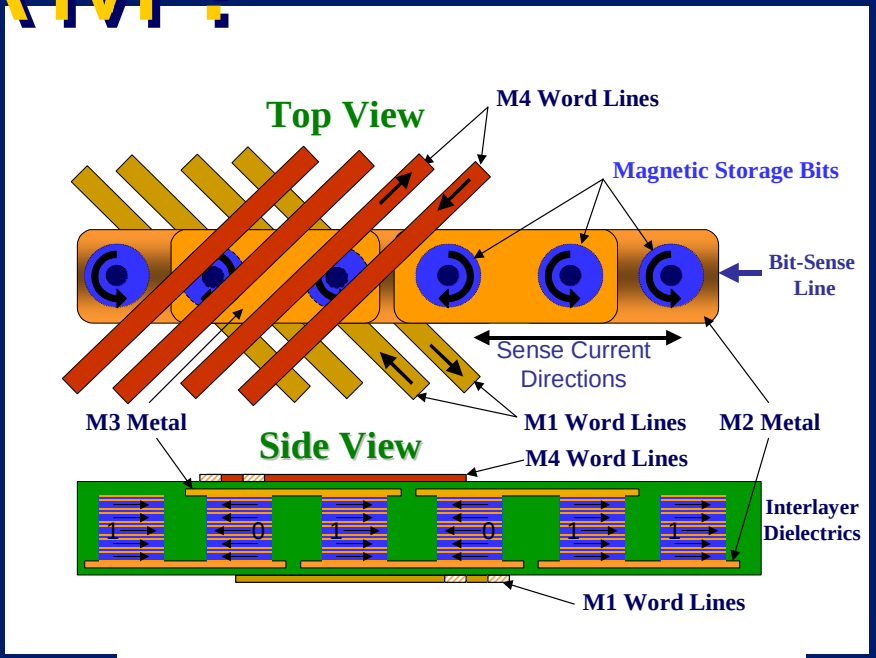


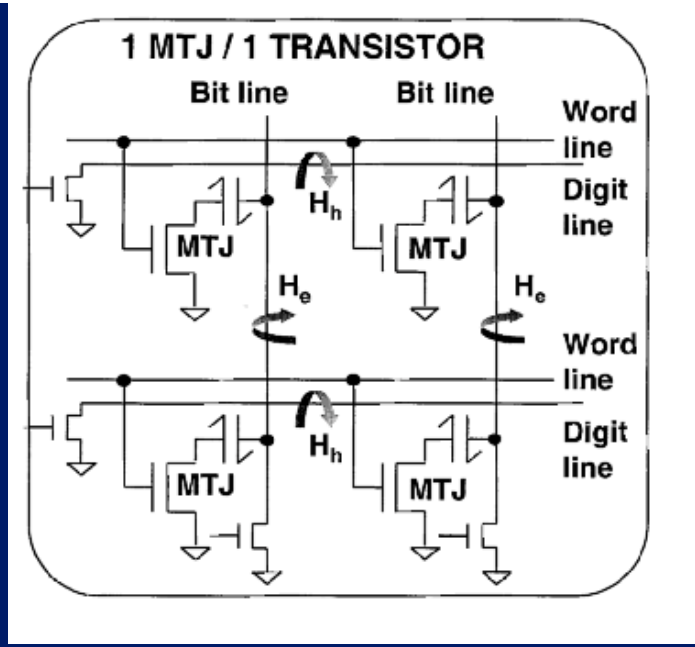
Memory Technologies Comparison



What Is MRAM?

- Operation
  - Cell is 1 MJT + 1 Transistor
  - Electric current switches the magnetic polarity
  - Change in magnetic polarity sensed as resistance change
- Attributes
  - Non-Volatile
  - High Density
  - Non Destructive Read
  - Low Voltage & Low Power
  - Write = Read Speed, < 50 nsec
  - Unlimited R/W Endurance
  - Material compatibility with CMOS a key challenge

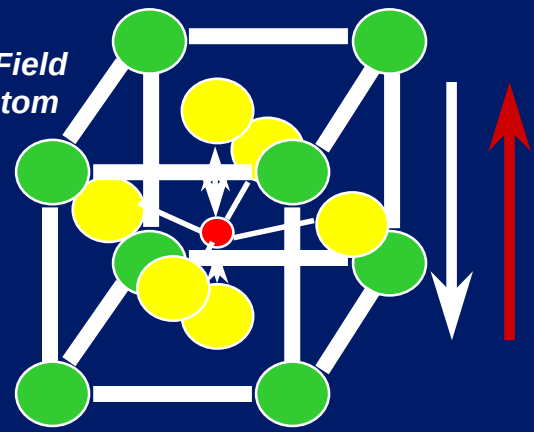




What Is FeRAM?

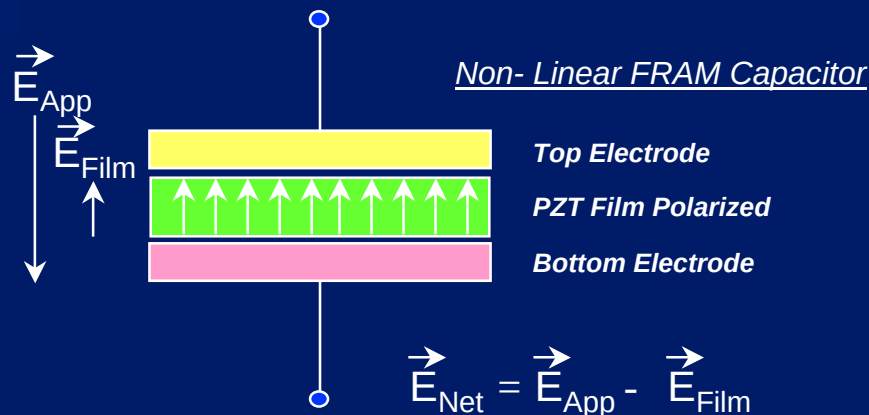
- Operation
  - Selected crystalline materials have bi-stable center atom
  - Data is stored by applying an voltage to polarize the internal dipoles “Up” or “Down”
  - Non-Linear FRAM Read Capacitor
- Attributes
  - Non-Volatile
  - Larger Cell Size
  - “Fast” Random Read Access
  - Fast Write with very low power consumption
  - Destructive read, limited read and write cycles

Applied Electric Field Moves Center Atom



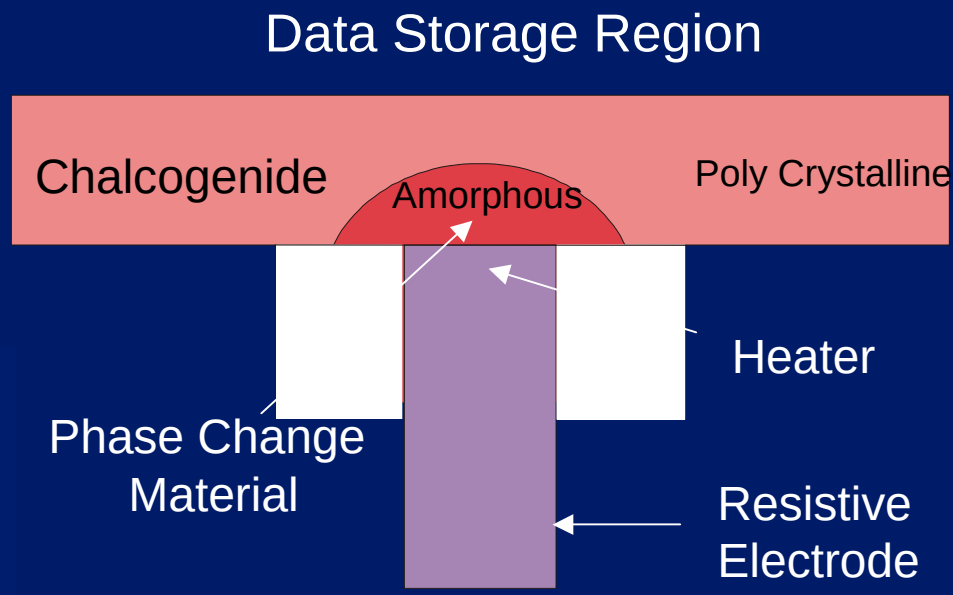
Perovskite Crystal Unit Cell
PZT (PbO, ZrO_2, TiO_2) Lead-Zirconate-Titanate

- Tetra/Pentavalent Atom
- Di/Monovalent Metal Atoms
- Oxygen Atoms



What Is OUM?

- Operation
  - Chalcogenide material alloys used in re-writable CDs and DVDs
  - Electrical energy (heat) converts the material between crystalline (conductive) and amorphous (resistive) phases
  - Cell reads by measuring resistance



- Attributes
  - Non-volatile
  - High density
  - Non-destructive read
  - Low voltage and low power
  - ~1012 write/erase cycles
  - Easy to integrate w/ logic

Technology Comparison

MRAM	FeRAM	OUM
Fastest Read and Write, Unlimited Cycles	Fast Read and Write, 10^{12} cycles	Fast Read and Write, 10^{12} cycles
Non Destructive Read	Destructive Read	Non Destructive Read
Special Process	Special Process	“Bolt on” Process
Larger Cell Size	Larger Cell Size	Smaller Cell Size

Agenda

- Scaling trend of ETOX® NOR Flash
- Multi-level and multi-bit technologies
- Internet on a chip technology
- Next generation memory technologies
- Ovonics unified memories for code + data storage
- Summary

OUM in 1970

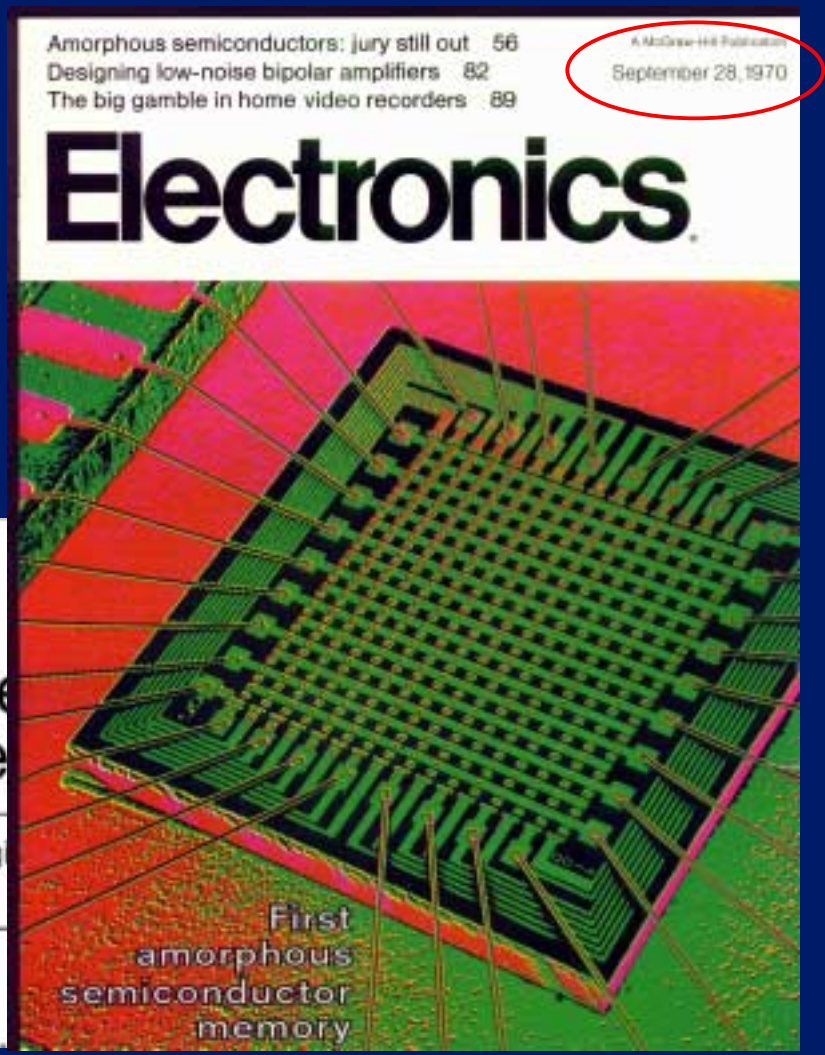
- Chalcogenide memories have been studied for > 30 years

Amorphous semiconductors Part I

Nonvolatile and reprogramable
the read-mostly memory is he

Integrated arrays combine amorphous and crystalline technologi
new memories could help realize promise of microprograming

By R. G. Neale and D. L. Nelson, *Energy Conversion Devices Inc., Troy, Mich.*
Gordon E. Moore, Intel Corp., *Mountain View, Calif.*

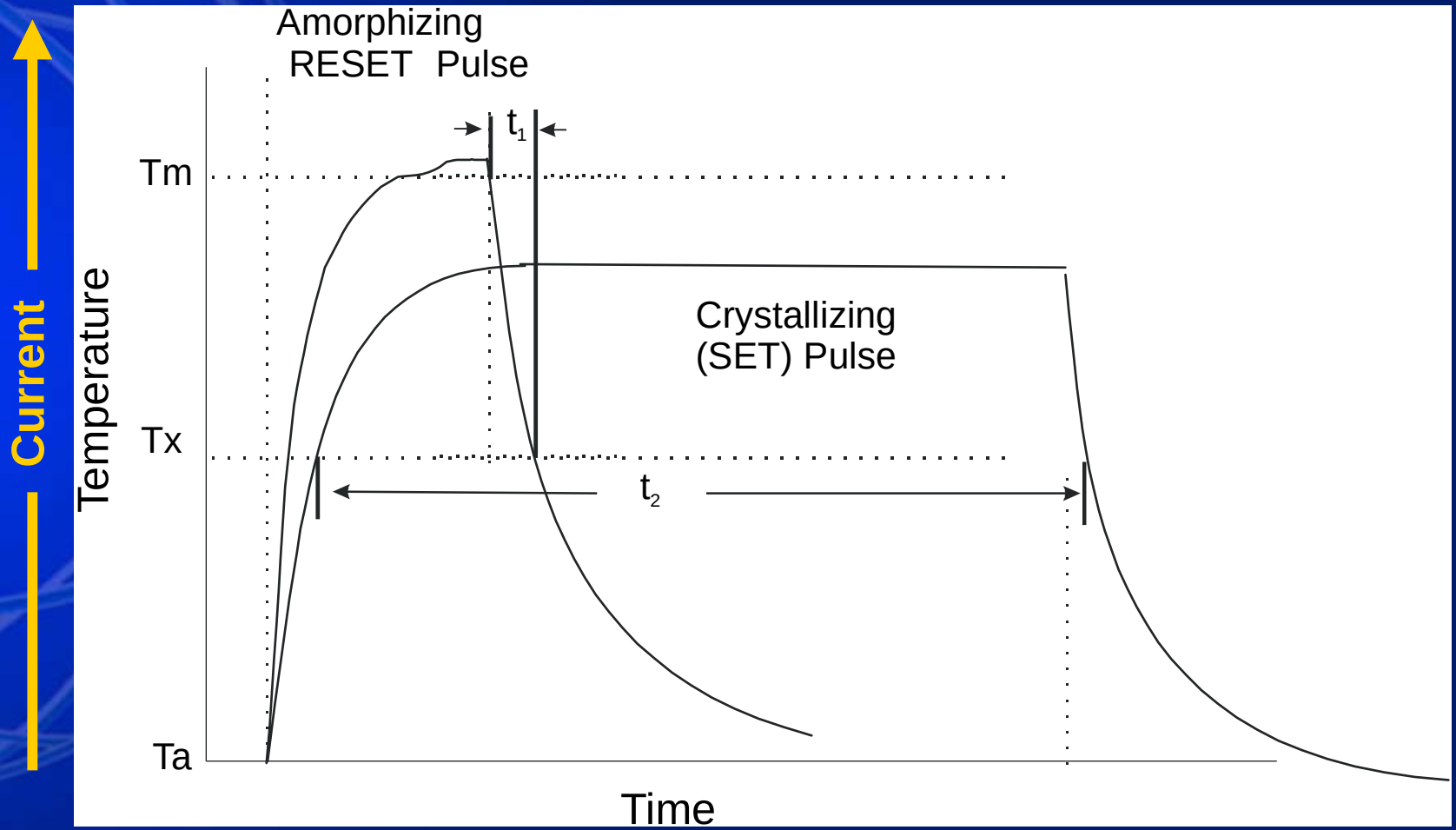


Why OUM Now?

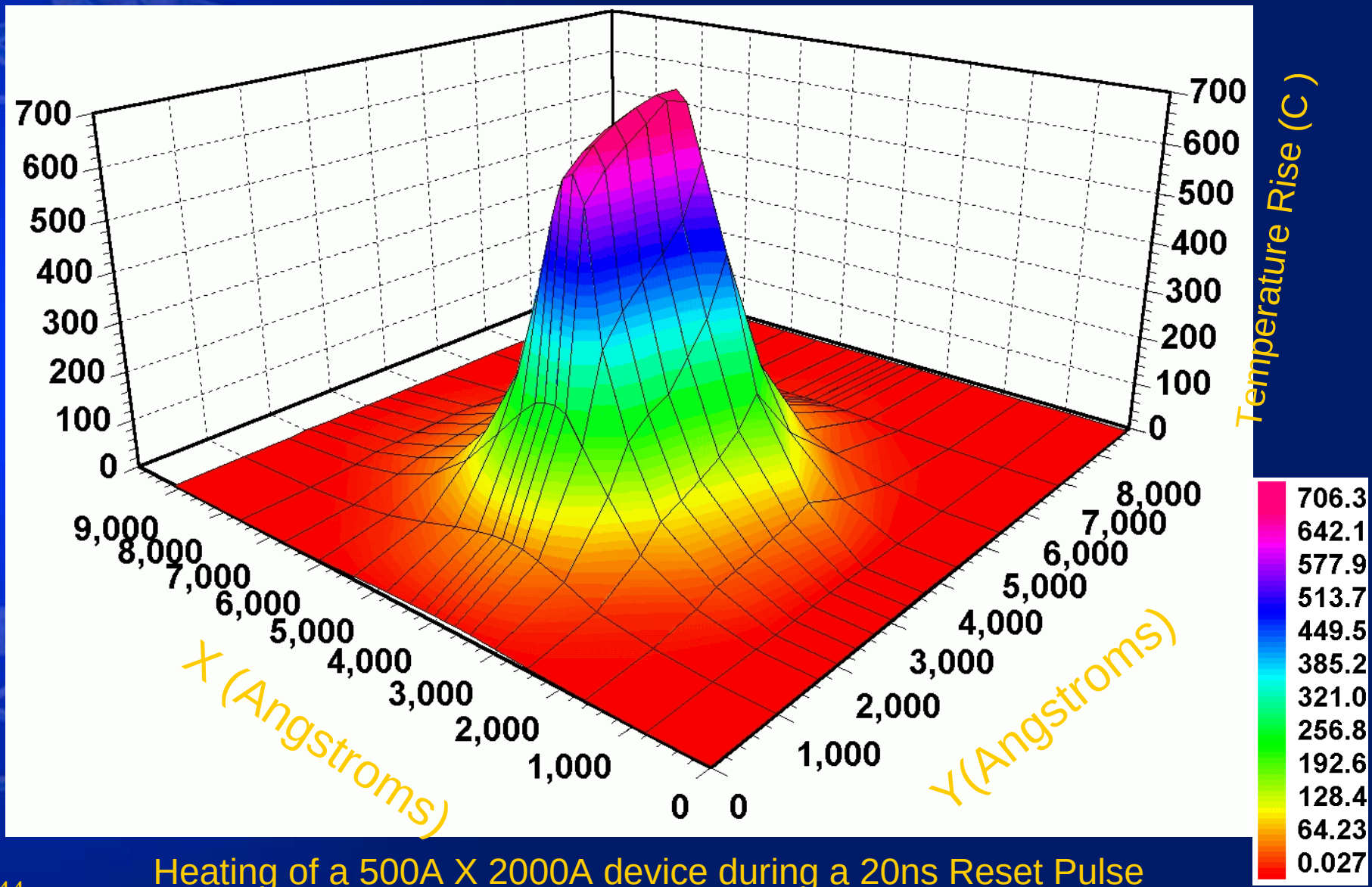
- Material technologies have benefited from 30 years of silicon manufacturing learning
  - High purity, thin film material can be prepared routinely
- Significant chalcogenide material improvement has lead to successful CD-RW and DVD-RW products
- New cell physics understanding leading to new cell structure design

Current Memory Structure

Basic Device Operation

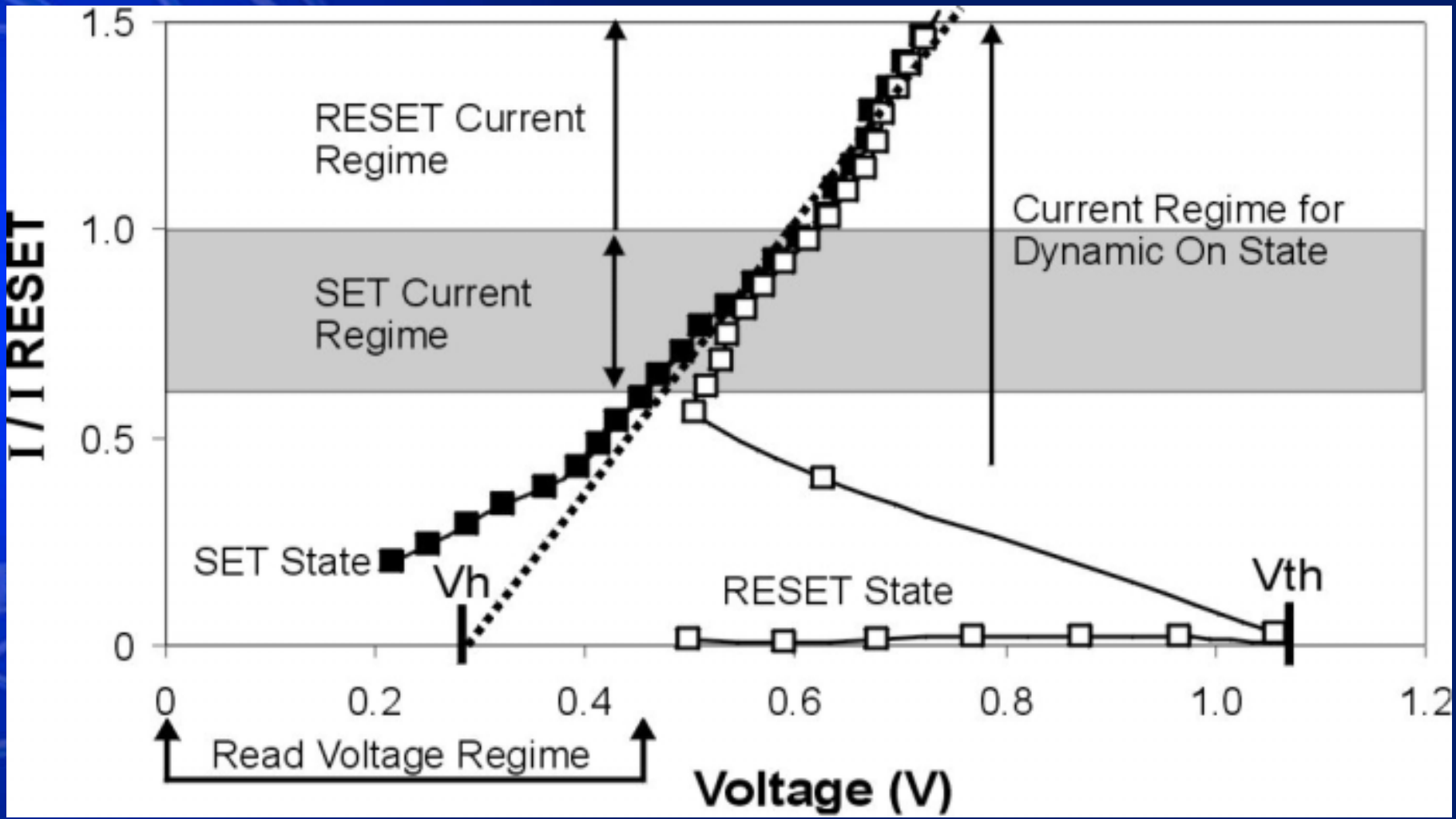


3D Temperature Profile of Heating

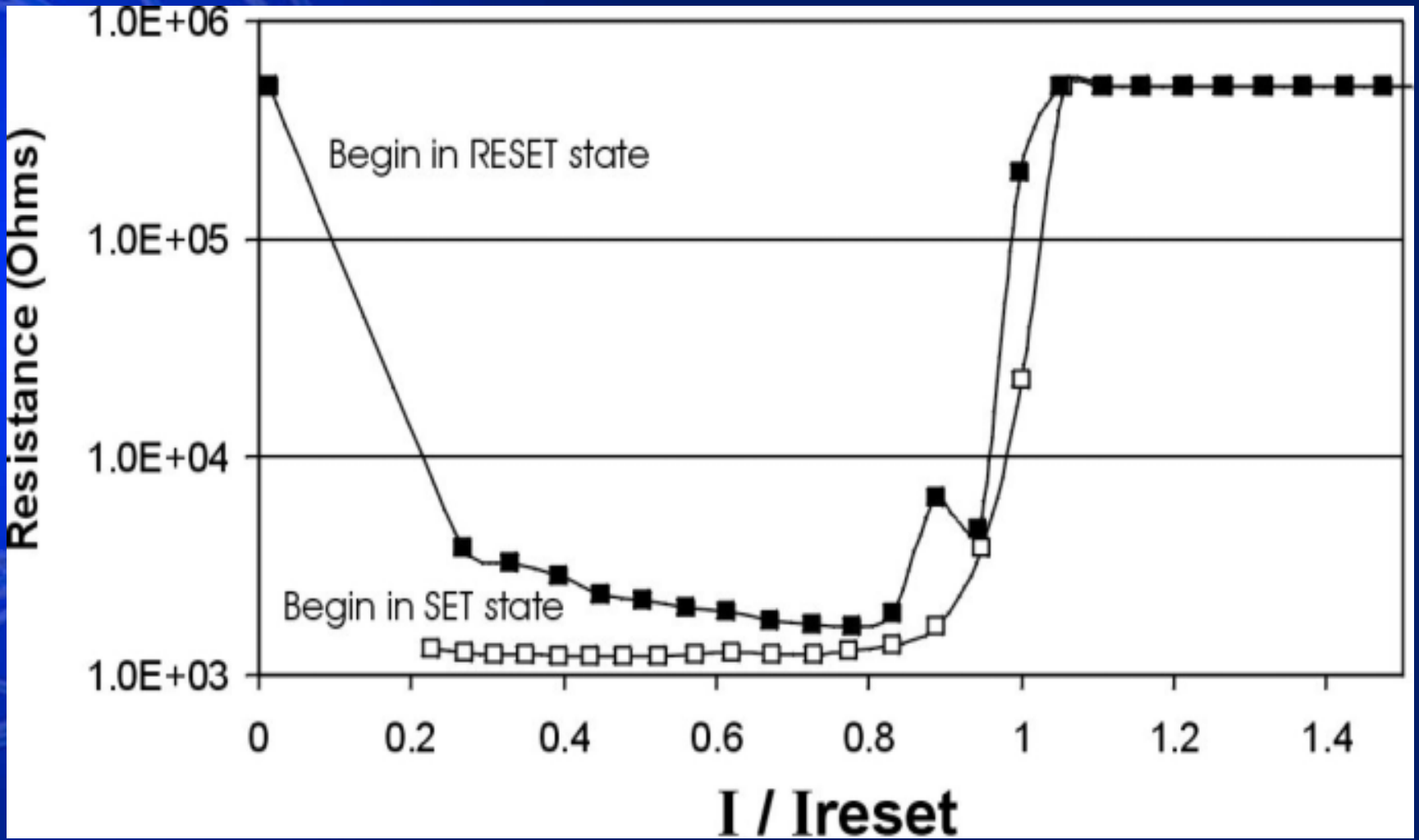


Heating of a 500A X 2000A device during a 20ns Reset Pulse

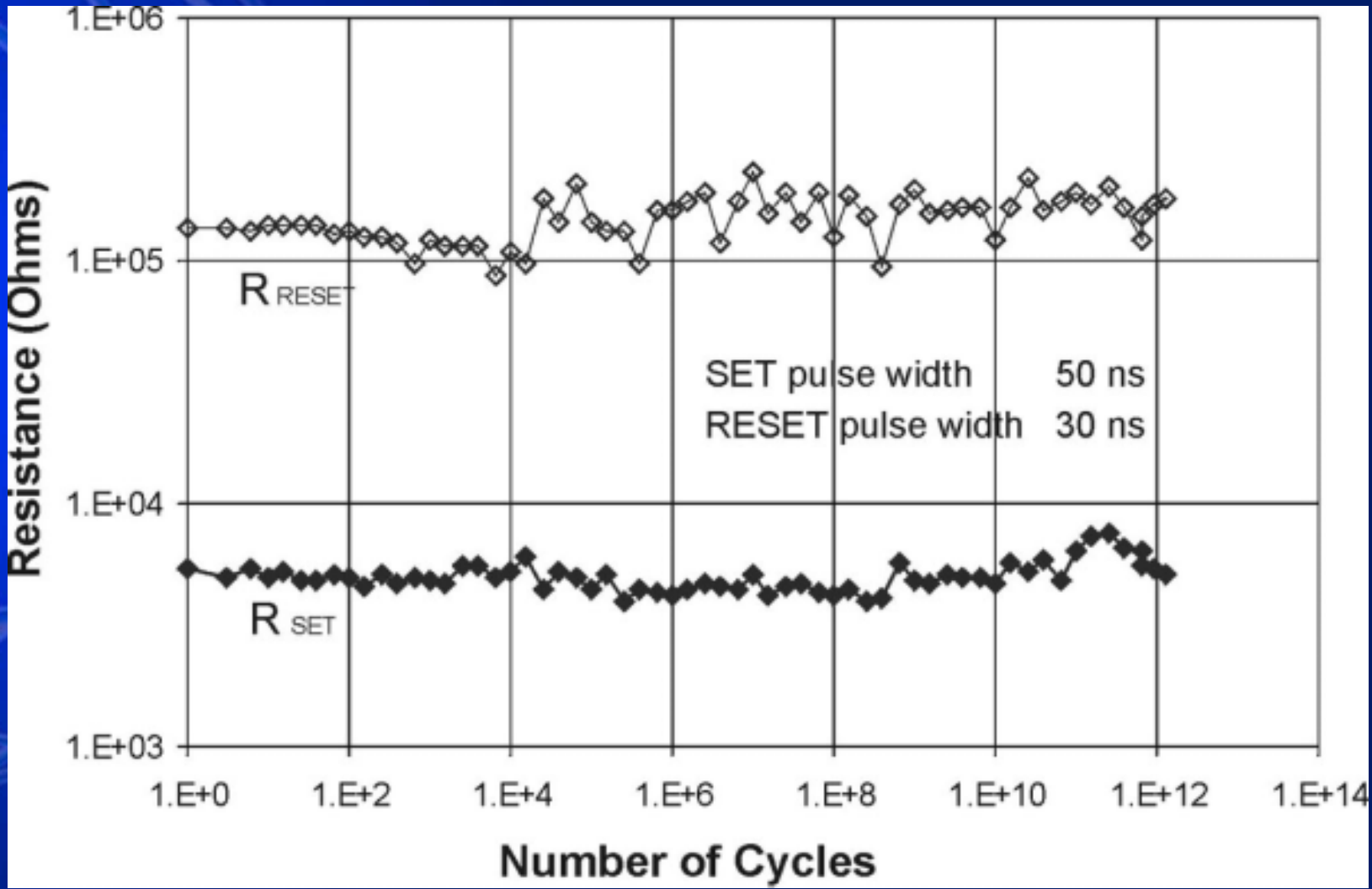
IV Curve of Chalcogenide Element



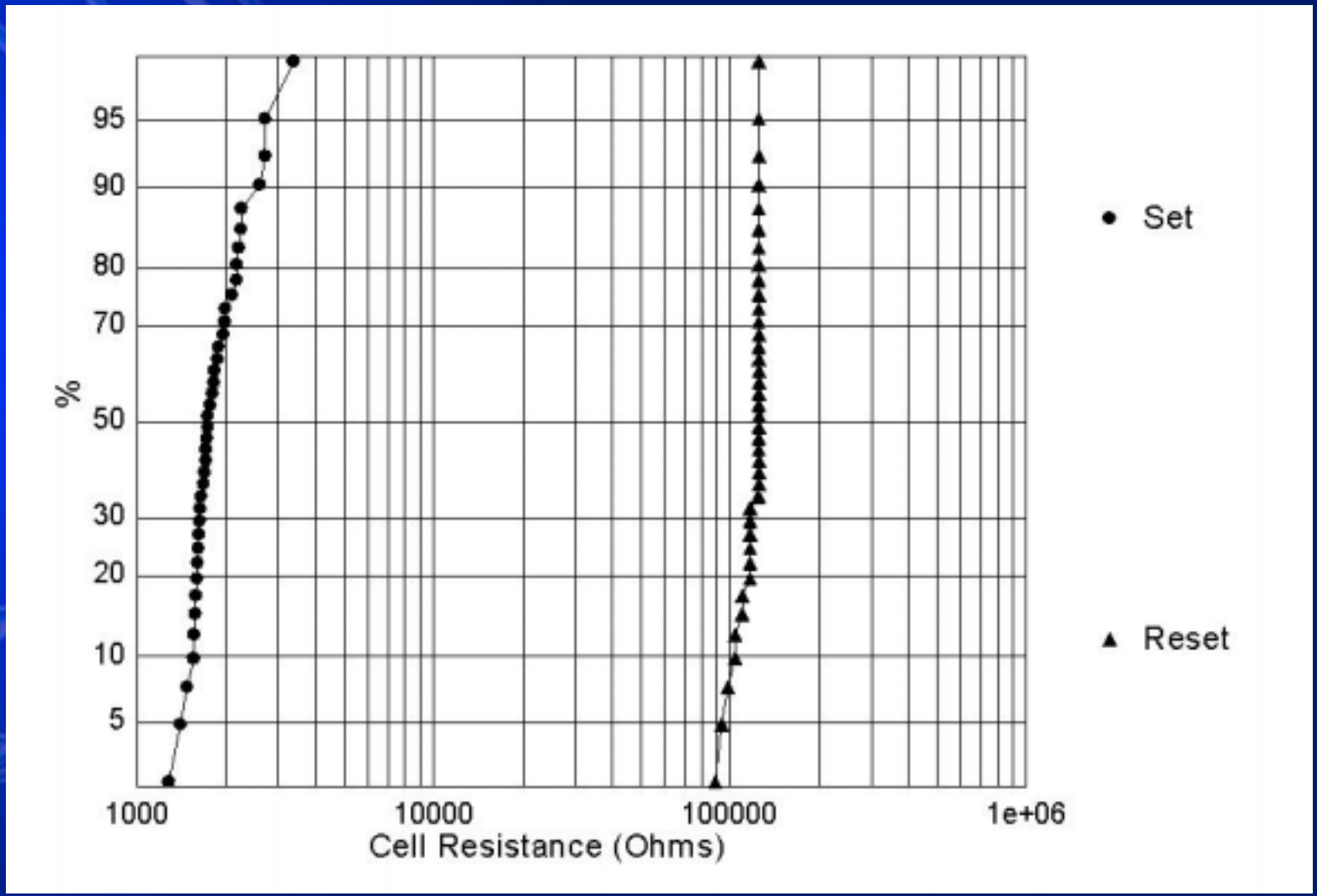
R_{set} and R_{reset} as Function of Cell Current



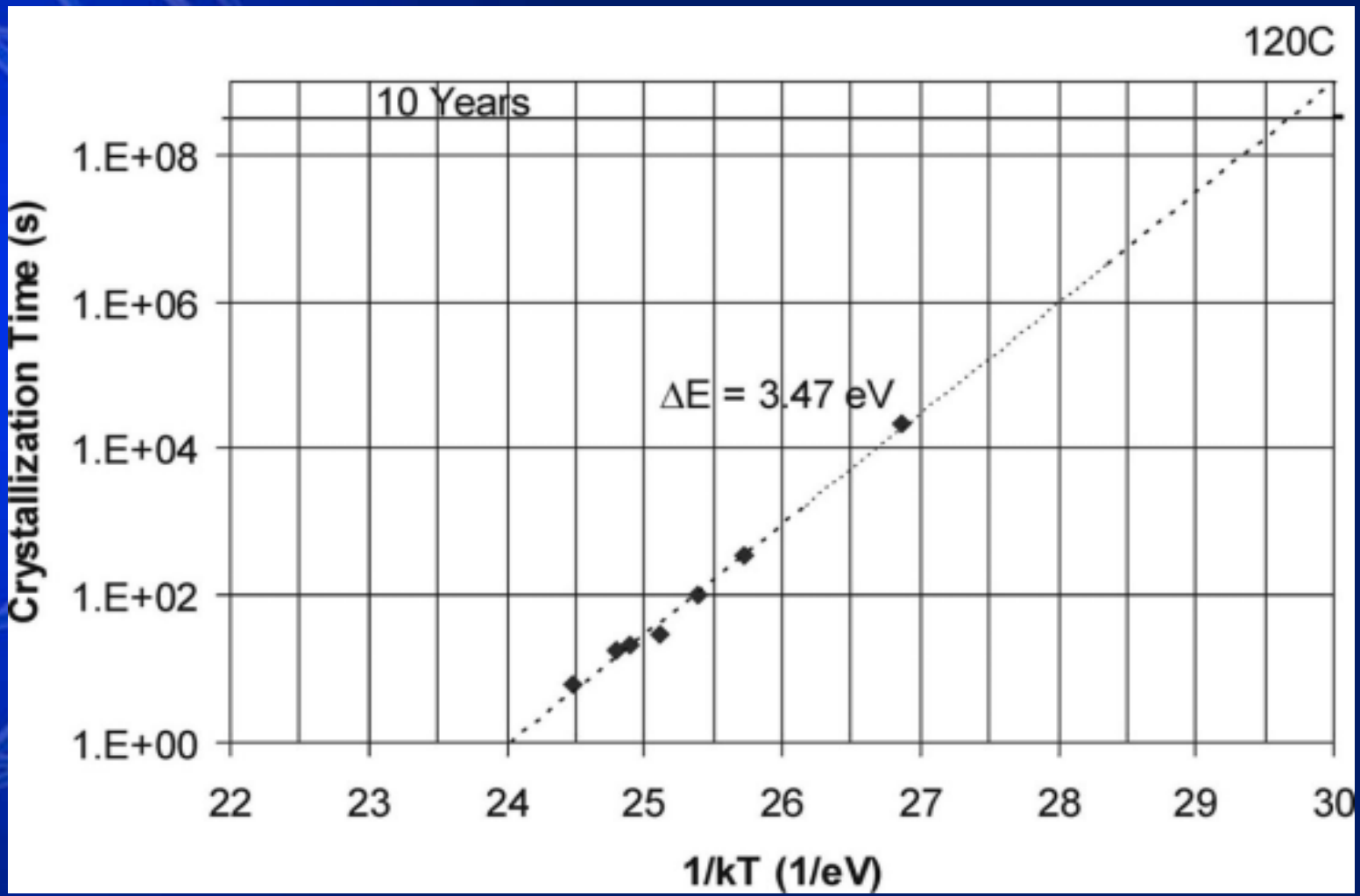
R_{set} and R_{reset} as Function of Cycles



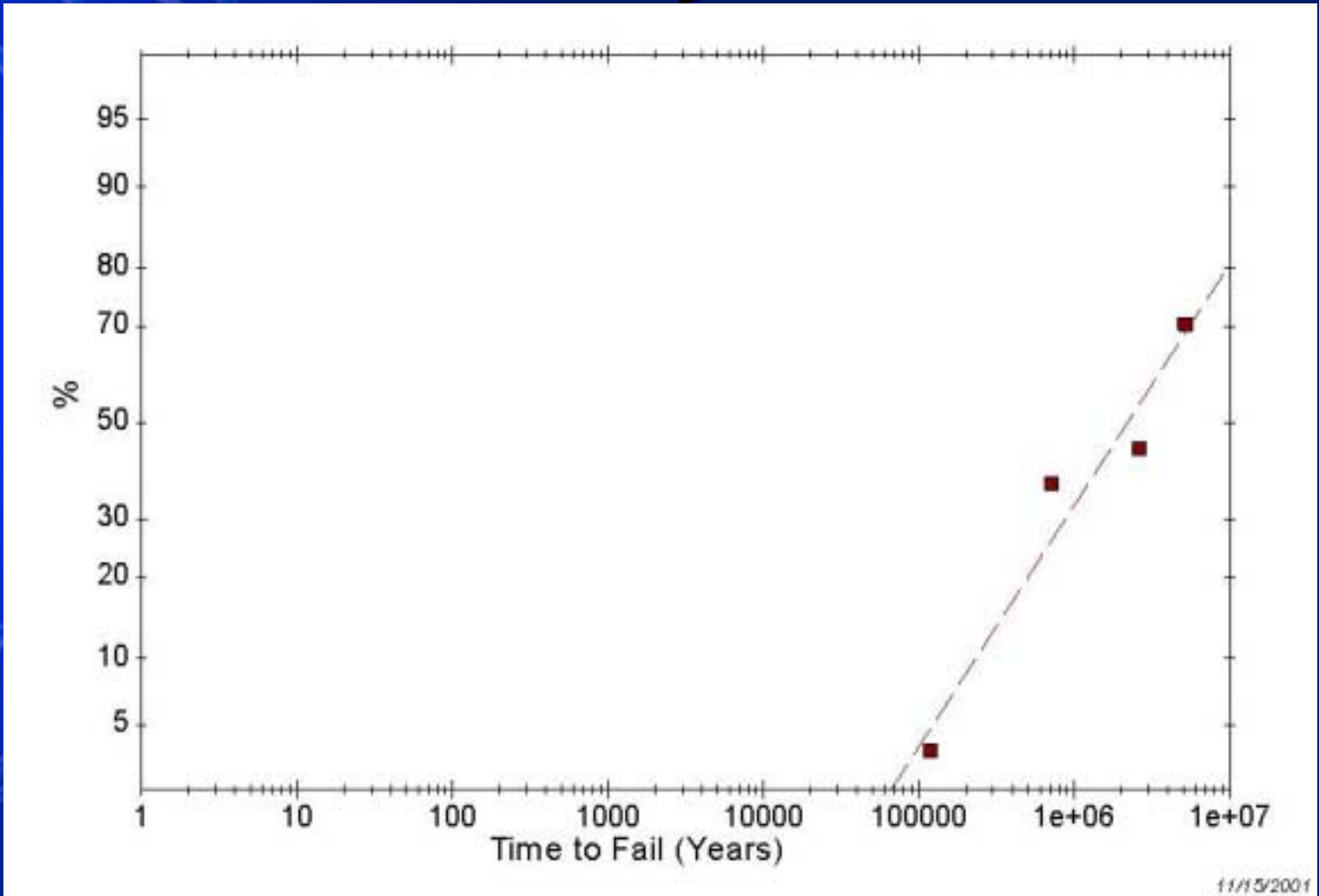
R_{set} and R_{reset} distribution after 10^7 cycles



Intrinsic Retention Characteristics



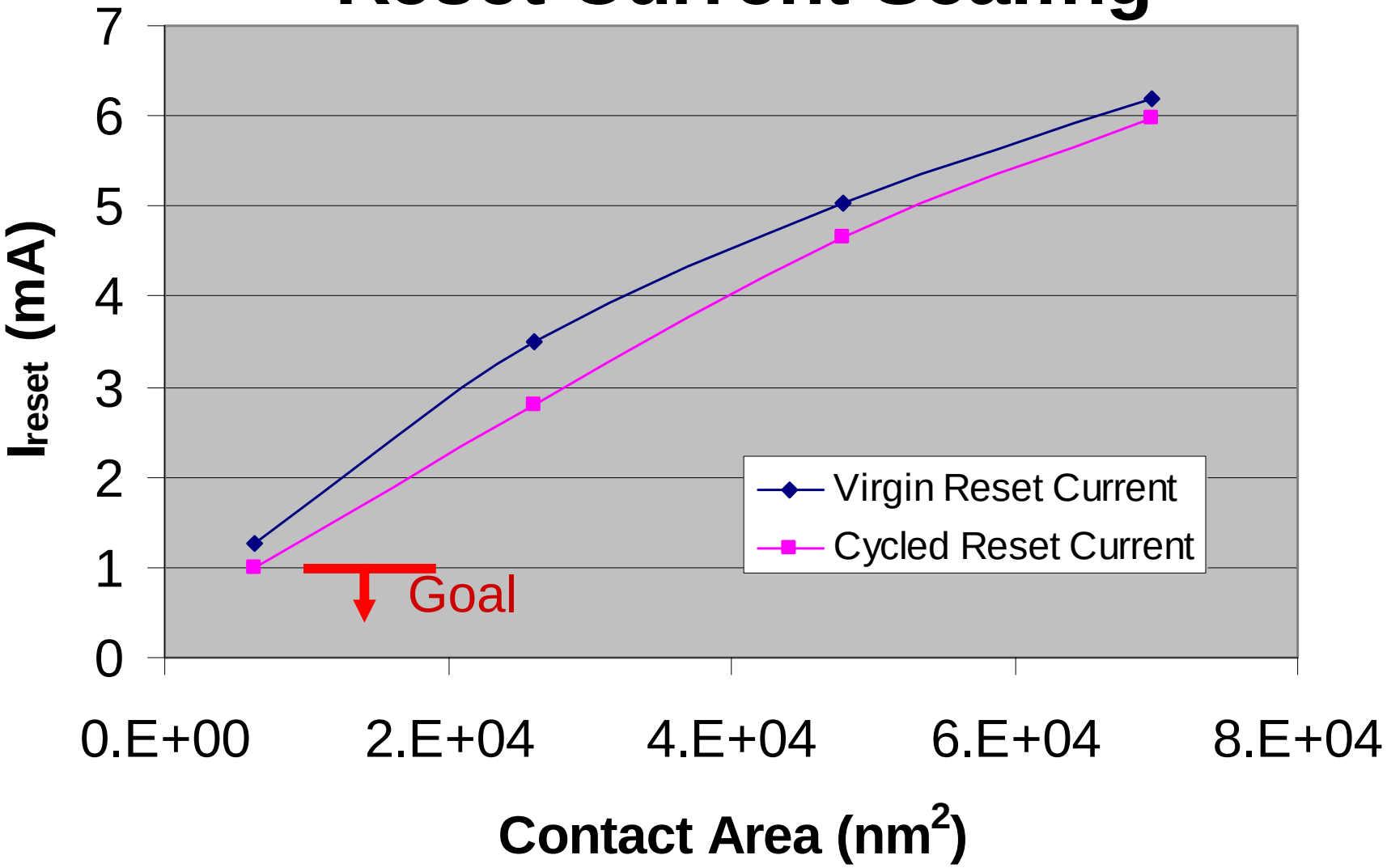
Failure Rate at 70ºC after 10^7 Cycles



Scaling

- Set and reset currents scale with the contact area; switching observed down to the smallest dimensions
- Thermal proximity is a concern: simulation showed capability down to 65 nm node, new structure and new material will extend to smaller geometries

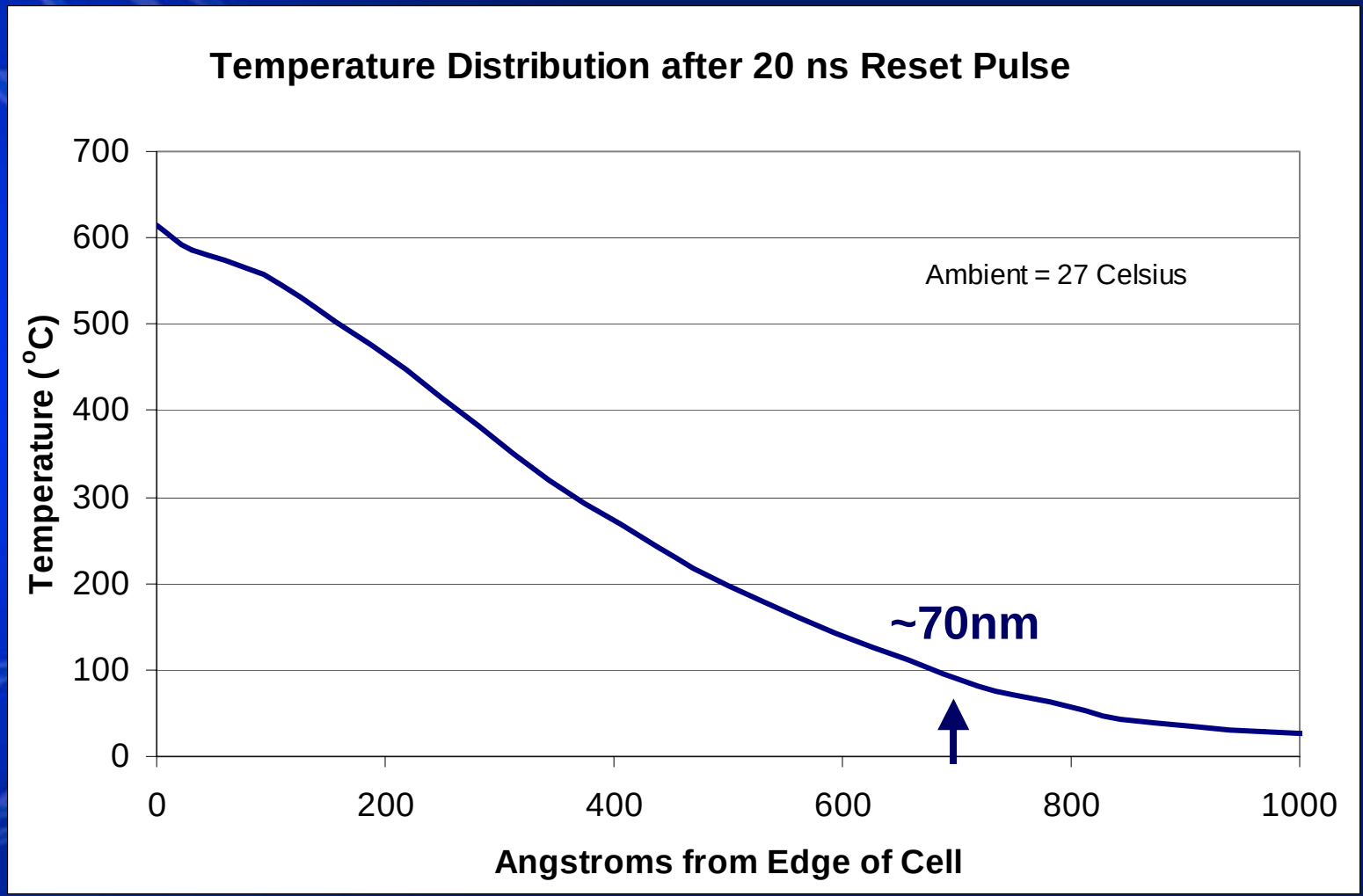
Reset Current Scaling



Scaling

- Set and reset currents scale with the contact area; switching observed down to the smallest dimensions
- Thermal proximity is a concern: simulation showed capability down to 65 nm node, new structure and new material will extend to smaller geometries

Temperature vs Radial Distance
For a Scaled Device



Cost Adder To Standard Process

- Chalcogenide material compatible with standard silicon processing
- Cell structure added after transistor formation before contact and interconnect
  - Standard metal process temperature has no impact on cell characteristics
- 3V transistor required, standard in most processes
- Minimal incremental process steps “bolt on” to standard process

Agenda

- Scaling trend of ETOX NOR Flash
- Multi-level and multi-bit technologies
- Internet on a chip technology
- Next generation memory technologies
- Ovonics unified memories for code + data storage
- Summary

Summary

- Current ETOX® NOR Structure Scales to 65 nm node, new innovation will take it further
- Continued scaling enables integration capability for internet on a chip
- Many candidates for next generation non-volatile memory technologies
  - New market and new business opportunities
- OUM shows promise for low cost XIP "code + data" memory solutions